PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-324125
(43)Date of publication of application : 25.11.1994

(51)Int.Cl. G01R 31/318
G11C 29/00

(21)Application number : 05-114781
(22)Date of filing : 17.05.1993

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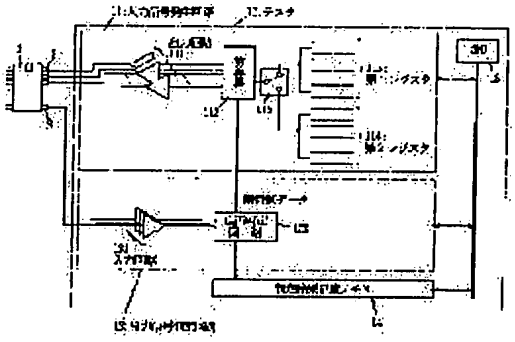
(54) TESTING DEVICE FOR SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To provide a test device for semiconductor device capable of precisely testing the quality of the characteristic of a semiconductor device at high speed regardless of the characteristic of the semiconductor device.
CONSTITUTION: In a first test area which is a part of the whole test area of a semiconductor memory device 1, a prescribed data outputted from an input signal generating circuit 11 is stored in the semiconductor memory device 1, the quality judgment of the read data is conducted by an output signal judging means 12, and the result is outputted to a judgment result storing memory 14. On the basis of the judgment result stored in the judgment result storing memory 14, a CPU 13 determines test conditions including the test condition of a boundary point where the judgment result is changed to good or bad quality. According to the test conditions, the test to the whole test area of the semiconductor memory device 1 is carried out by use of the input signal generating circuit 11 and the output signal judging circuit 12 to judge the quality of the characteristic.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平6－324125

(43)公開日　平成６年(1994)11月25日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｇ０１Ｒ　31/318				
Ｇ１１Ｃ　29/00	３０３　Ｆ	6866－5L		
		6912－2G	Ｇ０１Ｒ　31/ 28	Ａ

審査請求　未請求　請求項の数１　ＯＬ　（全 12 頁）

(21)出願番号　特願平5－114781

(22)出願日　平成５年(1993)５月17日

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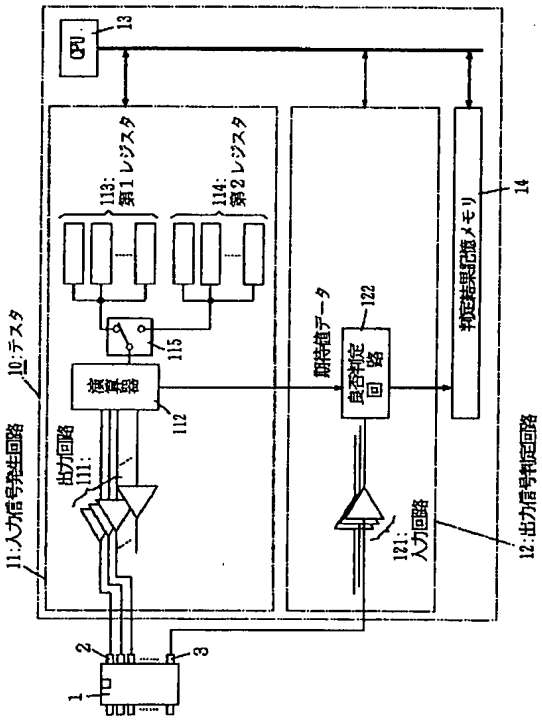
(54)【発明の名称】　半導体装置の試験装置

(57)【要約】

【目的】　半導体装置の特性にかかわらず、高速かつ正確に半導体装置の特性の良否を試験することができる半導体装置の試験装置を提供する。

【構成】　半導体記憶装置１の全試験領域の一部である第１試験領域において、入力信号発生回路１１から出力する所定のデータを半導体記憶装置１に記憶させ、読出したデータを出力信号判定回路１２が良否判定を行ない、その良否結果を判定結果記憶メモリ１４へ出力する。ＣＰＵ１３は判定結果記憶メモリに記憶されている判定結果を基に、判定結果が良または不良に変化する境界点の試験条件を含む試験条件を決定する。この試験条件により入力信号発生回路１１および出力信号判定回路１２を用いて半導体記憶装置１の全試験領域に対する試験を行ない、特性の良否判定を行なう。



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【特許請求の範囲】

【請求項１】　複数の試験条件に対する半導体装置の特性の良否について試験を行なう半導体装置の試験装置であって、

前記半導体装置の全試験領域の一部である第１試験領域において、前記複数の試験条件に対する前記半導体装置の特性の良否について試験を行なう第１試験手段と、

前記第１試験手段により得られた特性の良否結果を基に、少なくとも前記特性の良否が変化する第１試験条件を含み、前記複数の試験条件の一部である第２試験条件を決定する決定手段と、

前記半導体装置の全試験領域において、前記決定手段により決定された第２試験条件に対する前記半導体装置の特性の良否について試験を行なう第２試験手段とを含む半導体装置の試験装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、複数の試験条件に対する半導体装置の特性の良否について試験を行なう半導体装置の試験装置に関し、特に、複数の試験条件を連続的に変化させ、良否判定結果をマトリックス状に表示するシュムプロット図を作成する半導体装置の試験装置に関するものである。

【０００２】

【従来の技術】半導体技術の進歩により、半導体装置の高集積化が達成され、たとえば、半導体記憶装置の記憶容量はここ数年で飛躍的に増大している。このような大記憶容量を有する半導体装置に対してすべての試験領域の特性の良否について試験を行なおうとすると、記憶容量の増大に伴い試験時間も飛躍的に増大する。このような背景の下、短時間でかつ正確な特性の良否結果を判定する半導体装置の試験装置の開発が強く望まれている。

【０００３】以下、従来の半導体装置の試験装置（以下テスタと略す）について図面を参照しながら説明する。図１０は、従来のテスタの要部の構成を示すブロック図である。

【０００４】図１０において、テスタ２０は、入力信号発生回路２１、出力信号判定回路２２、ＣＰＵ（中央演算処理装置）２３を含む。ＣＰＵ２３は、入力信号発生回路２１および出力信号判定回路２２と接続され、各部の動作を制御する。入力信号発生回路２１はＣＰＵ２３から出力される動作指令により、所定の試験用データを作成し半導体記憶装置１の信号入力ピン２等を介して試験用データを半導体記憶装置１へ出力する。試験用データとしては、半導体記憶装置１内のメモリセルの番地を指定するアドレスデータ、そのメモリセルに格納されるセルデータ、半導体記憶装置１の書込、読出等の各動作を制御する制御データ等から構成される。ここでは、本発明の趣旨とは直接関係のないセルデータ、制御データ等の発生回路等は図示および説明を省略し、アドレスデータについて以下に詳細に説明する。

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【０００５】入力信号発生回路２１は、出力回路２１１、演算器２１２、レジスタ２１３を含む。レジスタ２１３は演算器２１２と接続され、アドレスデータの作成に必要なデータ、たとえば、半導体記憶装置１の全試験領域のアドレスの最大値、最小値等が予め記憶されており、ＣＰＵ２３からの動作指令に応じて演算器２１２へ所定のデータを出力する。演算器２１２は出力回路２１１と接続され、レジスタ２１３から出力されたデータを基に所定のアドレスデータを作成し、出力回路２１１へ出力する。出力回路２１１は半導体記憶装置１の信号入力ピン２と接続され、入力されたアドレスデータを半導体記憶装置１へ入力する。半導体記憶装置１は入力されたアドレスデータを基に所定のメモリセル内に別途転送されているセルデータを記憶する。

【０００６】次に、半導体記憶装置１は書込まれたセルデータを読出し、信号出力ピン３を介して出力信号判定回路２２へ出力する。出力信号判定回路２２は、入力回路２２１、良否判定回路２２２を含む。半導体記憶装置１から出力されたセルデータは入力回路２２１を介して良否判定回路２２２へ入力される。良否判定回路２２２は、演算器２１２と接続され、演算器２１２より、入力信号発生回路２１が記憶させたセルデータを表わす期待値データが入力される。良否判定回路２２２は、期待値データと読出されたセルデータとを比較し、特性の良否を判定する。判定結果はＣＰＵ２３へ出力され、ＣＰＵ２３は、この判定結果を基に、表示装置または印刷装置（図示省略）へ試験結果を表示し、半導体記憶装置１の特性の良否について知ることが可能となる。

【０００７】次に、上記のように構成されたテスタ２０を用いた半導体記憶装置の特性試験の方法について説明する。半導体記憶装置の特性試験の１つにシュムプロットがある。シュムプロットとは、数種類の試験条件パラメータ（たとえば、電源電圧、各種信号の入力タイミング等）のうち２つの試験条件パラメータまたは３つの試験条件パラメータを所定の間隔で変化させた複数の試験条件で試験を実施し、その良否判定結果を２次元または３次元のマトリックス状にプロットし、半導体記憶装置の特性を試験するものである。

【０００８】図１１に、シュムプロット図の一例を示す。試験条件パラメータとしては、半導体記憶装置に与える電源電圧および半導体記憶装置から出力されるデータの良否判定を行なう時間を用いている。図１１では、電源電圧を縦軸にとり、５．５Ｖ～４．５Ｖまで０．１Ｖ刻みに１１ポイントの電源電圧を変化させ、出力されるデータの良否判定を行なう時間を横軸にとり、９５ｎｓ～１１０ｎｓまで１ｎｓ刻みに１６ポイントの試験条件を変化させている。この結果、１１ポイント×１６ポイント＝１７６ポイントの各試験条件で試験が実施され、試験結果が“良”であればそのポイントに“＊”を

表示し、“不良”であれば空白のままにしている。図１１に示すシュムプロット図として表示することにより、複数の試験条件に対する試験結果の良否を一目で認識することが可能となる。

【０００９】次に、上記のシュムプロット図を作成するために各試験条件を実施する順序について説明する。図１２は、各試験条件を実施する順序を示す図である。図１２に示すように、各試験条件は矢印の示すような順序で実施される。まず、縦軸の第２試験パラメータの条件を固定した後、横軸の第１試験パラメータを所定の間隔で変化させながら試験を実施し、横軸のすべての試験条件に対して試験が終了した後、縦軸の第２試験パラメータの試験条件を所定の間隔で変化させ、同様に試験を行ない、すべての試験条件について試験が終了するまで繰返すものである。

【００１０】次に、図１２に示すシュムプロット図を作成する従来のテスタの動作について以下に説明する。図１３は、従来のテスタの動作を説明するフローチャートである。図１３に示すフローチャートは、プログラムとしてＣＰＵ２３内の記憶装置に予め記憶され、必要に応じてＣＰＵ２３がそのプログラムを実行することにより実現される。

【００１１】まず、ステップＳ２１において、ＣＰＵ２３は縦軸の試験条件の初期値を設定する。

【００１２】次に、ステップＳ２２において、ＣＰＵ２３は横軸の試験条件の初期値を設定する。

【００１３】次に、ステップＳ２３において、ＣＰＵ２３は設定された試験条件で試験を行なうように入力信号発生回路２１および出力信号判定回路２２に指令し、試験を実行する。

【００１４】次に、ステップＳ２４において、出力信号判定回路２２は試験結果の良否を判定し、判定結果をＣＰＵ２３へ出力する。ＣＰＵ２３は入力された良否判定結果を基に、試験結果が“良”であればステップＳ２５へ移行し、“不良”であればステップＳ２６へ移行する。

【００１５】次に、ステップＳ２５において、ＣＰＵ２３はシュムプロット図の所定の試験条件を示す位置に“＊”を表示する。一方、“不良”と判定された場合はステップＳ２５をスキップしているので、シュムプロット図上には何も表示されない。

【００１６】次に、ステップＳ２６において、ＣＰＵ２３は横軸の試験条件すべてに対して試験が終了したか否かを確認する。試験が終了していなければ、次の横軸の試験条件を設定するためステップＳ２８へ移行する。試験が終了していれば次の縦軸の試験条件を設定するためステップＳ２７へ移行する。

【００１７】次に、ステップＳ２６において、横軸の試験条件が終了していないと判断され、ステップＳ２８に移行した場合、ＣＰＵ２３は横軸の試験条件を次の試験条件に変更し、ステップＳ２３へ移行し、以降の処理を繰返す。

【００１８】一方、ステップＳ２６において横軸の試験条件すべてについて終了したと判断された場合、ステップＳ２７において、ＣＰＵ２３は縦軸のすべての試験条件に対する試験が終了したか否かを確認する。縦軸の試験条件が終了していなければ、次の試験条件を設定するためステップＳ２９へ以降し、終了していれば、すべての試験条件に対する試験が終了しているので処理を終了する。

【００１９】次に、ステップＳ２７において縦軸の試験条件が終了していないと判断され、ステップＳ２９へ移行した場合、ＣＰＵ２３は横軸の試験条件として初期値を設定する。

【００２０】次に、ステップＳ３０において、ＣＰＵ２３は縦軸の試験条件を次の試験条件に変更し、ステップＳ２３へ移行し、以降の処理を続ける。

【００２１】以上の動作により、テスタ２０は、図１２に示す試験条件の順序ですべての試験条件に対する試験を実施し、各試験条件に対する良否判定結果を表わすシュムプロット図を作成することが可能となる。

【００２２】次に、上記のようにすべての試験条件に対する試験を行ないシュムプロット図を作成するのではなく、所定の順序で試験を行なうことにより試験時間を短縮することができるバイナリサーチ手法によるシュムプロット図の作成について以下に説明する。図１４は、従来のテスタを用いたバイナリサーチ手法による試験順序を説明する図である。

【００２３】図１４に示すように、横軸に第１試験パラメータをとり、縦軸に第２試験パラメータをとる。まず、縦軸の第２試験パラメータを所定の条件に固定した後、横軸の第１試験パラメータの左端の試験条件で試験を行なう。次に、同じ第２試験パラメータに対して、横軸の第１試験パラメータの右端の試験条件で試験を行なう。試験結果、矢印１で示す試験条件の結果が“不良”（空白）、矢印２で示す試験条件の結果が“良”（“＊”）となり、両者の試験判定結果が異なる場合は両者の中間ポイントを試験する。ここでは、中間の試験条件として、たとえば、矢印３で示す試験条件で次の試験を行なう。このとき、試験結果が“良”である場合は、矢印１で示す試験条件と矢印３で示す試験条件との間の試験条件たとえば、矢印４で示す条件で次の試験を行なう。矢印４に示す試験条件での試験結果が“不良”である場合は矢印４で示す試験条件と矢印３で示す試験条件の間である矢印５で示す試験条件で次の試験を行なう。矢印５で示す試験条件の試験結果が“良”である場合、矢印４で示す試験条件と矢印５で示す試験条件との間が良／不良の境界点となるため、矢印５で示す試験条件の部分に“＊”をプロットする。

【００２４】以上に述べたように、バイナリサーチ手法

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は、異なる２つの試験条件で試験を行ない、試験結果が異なる場合、その間の試験条件で試験を行なうことにより、すべての試験条件に対して試験を行なうことなく、良／不良の境界点を特定することができるため、試験時間を短縮することが可能となる。たとえば、図１４では、９個の試験条件に対し、５個の試験条件で試験を行なうことにより、良／不良の境界点を特定することができ、試験時間は９分の５に短縮される。上記の処理を第２試験パラメータの各試験条件に対して試験を行なうことにより、全体の試験時間を同様に短縮することができ、高速にシュムプロット図を作成することが可能となる。

【００２５】次に、上記のバイナリサーチ手法による従来のテスタの動作について説明する。図１５は、バイナリサーチ手法による従来のテスタの動作を説明するフローチャートである。

【００２６】まず、ステップＳ３１において、ＣＰＵ２３は縦軸の試験条件として初期値を設定する。

【００２７】次に、ステップＳ３２において、ＣＰＵ２３はバイナリサーチ手法による試験実行を行なうサブルーチンを実行する。バイナリサーチ手法による試験実行のサブルーチンは以下のように処理される。

【００２８】まず、ステップＳ３５において、良否判定結果として“良”を示す試験条件Ｎと“不良”を示す試験条件Ｍとで試験を行なう。

【００２９】次に、ステップＳ３６において、試験条件Ｎと試験条件Ｍとの中間点の試験条件Ｌで試験を行なう。

【００３０】次に、ステップＳ３７において、中間点の試験条件Ｌにおける良否判定を行なう。判定結果が“不良”の場合ステップＳ４１へ移行し、“良”の場合ステップＳ３８へ移行する。

【００３１】ステップＳ３７で“良”と判定された場合、ステップＳ３８において、試験条件Ｎを試験条件Ｌに置換える。

【００３２】一方、ステップＳ３７において、“不良”と判断された場合、ステップＳ４１において、試験条件Ｍを試験条件Ｌに置換える。

【００３３】以上の処理により、試験条件Ｎと試験条件Ｍとの間に良／不良の境界点が存在することになる。

【００３４】次に、ステップＳ３９において、試験条件Ｎと試験条件Ｍが隣合う試験条件であるか否かを確認する。隣合う試験条件である場合は、良／不良の境界点が特定できるので、ステップＳ４０へ移行する。隣合う試験条件でなければ、良／不良の境界点は試験条件Ｎと試験条件Ｍとの間に存在する可能性があるので、ステップＳ３６へ移行し、中間点の試験条件Ｌについて再び試験を行なう。

【００３５】次に、ステップＳ４０において、良／不良の境界点となる“良”のポイントをプロットする。以上

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の処理により、すべての試験条件に対して試験を行なうことなく、良／不良の境界点となる試験条件を特定することができ、高速に、シュムプロット図を作成することが可能となる。

【００３６】

【発明が解決しようとする課題】上記のように従来のテスタは構成されているので、特性試験としてシュムプロットを採取するためには、縦軸および横軸に設定した全試験条件に対して試験を繰返す必要があり、試験時間が非常に長くなるという問題点があった。たとえば、１６Ｍｂｉｔの半導体記憶装置の場合、全試験領域を所定の試験条件で試験したとすると、約４．６時間を要し、非常に長大な時間が必要となっていた。また、この試験時間は、半導体記憶装置の容量の増加とともに飛躍的に増大するものであり、今後ますます大きな問題となることが予想される。

【００３７】また、試験時間を短縮する方法として開発されているバイナリサーチ手法においては、良／不良の境界点が複数以上存在する特性を示す半導体装置に対しては使用できないという問題点があった。図１６に、良（“＊”）／不良（空白）の境界が複数ある半導体記憶装置を試験した場合のシュムプロット図を示す。図１６に示すように、良／不良の境界が複数ある場合は、バイナリサーチ手法では、１つの境界しか検出しないため、その他の境界は無視されてしまう。図１７に、図１６に示す特性を有する半導体記憶装置をバイナリサーチ手法により試験した場合のシュムプロット図を示す。図１７から明らかなように、良／不良の境界は１つだけが検出され、その他の境界点は検出されていないので、全く間違った良否判定結果を表示してしまい、正確な評価を実現できないという問題があった。

【００３８】本発明は上記課題を解決するためのものであって、半導体装置の特性にかかわらず、高速かつ正確に半導体装置の特性の良否を試験することができる半導体装置の試験装置を提供することを目的とする。

【００３９】

【課題を解決するための手段】本発明の半導体装置の試験装置は、半導体装置の全試験領域の一部である第１試験領域において、複数の試験条件に対する半導体装置の特性の良否について試験を行なう第１試験手段と、第１試験手段により得られた特性の良否結果を基に、少なくとも特性の良否が変化する第１試験条件を含み、複数の試験条件の一部である第２試験条件を決定する決定手段と、半導体装置の全試験領域において、決定手段により決定された第２試験条件に対する半導体装置の特性の良否について試験を行なう第２試験手段とを含む。

【００４０】

【作用】本発明の半導体装置の試験装置においては、全試験領域の一部である第１試験領域において複数の試験条件すべてに対して半導体装置の特性の良否について試

験を行なうので、完全な良否試験結果を得ることができる。この試験結果を基に、特性の良否が変化する第１試験条件を含み、複数の試験条件の一部である第２試験条件を決定するので、第２試験条件は、すべての試験条件よりその数が少なく、必ず特性の良否が変化する試験条件を含んだ試験条件となる。この第２試験条件に対する半導体装置の特性の良否について全試験領域を試験する。

【００４１】

【実施例】以下、本発明の一実施例である半導体装置の試験装置（従来例と同様に以下テスタと称す）について図面を参照しながら説明する。図１は、本発明の一実施例のテスタの要部の構成を示すブロック図である。

【００４２】図１において、テスタ１０は、入力信号発生回路１１、出力信号判定回路１２、ＣＰＵ（中央演算処理装置）１３、判定結果記憶メモリ１４を含む。ＣＰＵ１３は、入力信号発生回路１１、出力信号判定回路１２、判定結果記憶メモリ１４とそれぞれ接続され、各部の動作を制御する。入力信号発生回路１１は、ＣＰＵ１３から出力される動作指令信号に応答して、試験用データを作成し、入力信号ピン２を介して半導体記憶装置１へ入力する。試験用データとしては、従来と同様に、半導体記憶装置１内のメモリセルの番地を指定するアドレスデータおよび所定のメモリセルに蓄えるセルデータ等から構成される。セルデータ等は従来のテスタと同様に半導体記憶装置１へ入力されるが、本発明の趣旨とは直接関係がないので、セルデータの発生回路等は図示を省略するとともにその説明を省略する。

【００４３】半導体記憶装置１は入力信号発生回路１１から出力された試験用データに基づき記憶したセルデータを読出し、信号出力ピン３を介して出力信号判定回路１２へ出力する。出力信号判定回路１２は入力されたセルデータと、入力信号発生回路１１から出力される期待値データとを比較し、良否の判定結果を判定結果記憶メモリ１４およびＣＰＵ１３へ出力する。判定結果記憶メモリ１４は出力信号判定回路１２から出力される良否の判定結果を記憶し、必要に応じてＣＰＵ１３へ出力する。

【００４４】入力信号発生回路１１は、出力回路１１１、演算器１１２、第１レジスタ１１３、第２レジスタ１１４、切換スイッチ１１５を含む。第１レジスタ１１３は、半導体記憶装置１のメモリ容量のすべてを試験するための入力信号を発生するのに必要なデータを蓄えている。たとえば、半導体記憶装置１の全試験領域に対応したアドレスの最大値、最小値等である。第２レジスタ１１４は、半導体記憶装置１の記憶容量の一部分のみを試験するための入力信号を発生するのに必要なデータを蓄えている。たとえば、試験領域の所定領域に対応したアドレスの最大値、最小値等である。切換スイッチ１１５は第１レジスタ１１３および第２レジスタ１１４と演

算器１１２との接続を切換える。つまり、半導体記憶装置１の全試験領域を試験する場合は、第１レジスタ１１３が指定され、全試験領域に対応したデータが演算器１１２へ出力される。また、試験領域の一部のみを試験する場合は第２レジスタ１１４が接続され、所定の試験領域に対応したデータが演算器１１２へ出力される。演算器１１２は、第１レジスタ１１３または第２レジスタ１１４から入力されたデータを基に所定のアドレスデータを作成し、出力回路１１１へ出力する。出力回路１１１は入力したアドレスデータを所定の波形に整形した後、信号入力ピン２を介して半導体記憶装置１へ出力する。上記のアドレスデータ以外の試験用データは従来のテスタと同様に作成され、半導体記憶装置１へ入力される。出力信号判定回路１２は、入力回路１２１、良否判定回路１２２を含む。入力信号発生回路１１から出力されたセルデータを記憶した半導体記憶装置１は記憶したセルデータを再び読出し、信号出力ピン３を介して入力回路１２１へ出力する。読出されたセルデータは入力回路１２１を介して良否判定回路１２２へ出力される。良否判定回路１２２には演算器１１２から記憶したセルデータを示す期待値データが出力され、この期待値データと、入力されたセルデータとを比較し、特性の良否を判定する。良否判定回路１２２は、良否の判定結果が全試験領域に対するものである場合は判定結果をＣＰＵ１３へ出力し、試験領域の一部である場合は判定結果記憶メモリ１４へ判定結果を出力する。判定結果記憶メモリ１４は試験領域の一部の良否の判定結果を記憶し、ＣＰＵ１３は記憶された判定結果から、特性が良または不良に変化する良／不良の境界点を識別する。ＣＰＵ１３は識別した境界点を基に、特性の良否が変化する試験条件を含んだ所定の試験条件を設定し、入力信号発生回路１１へその試験条件で全試験領域を試験するように指令する。

【００４５】次に、上記のように構成されたテスタの動作について詳細に説明する。図２は、テスタの動作を説明するフローチャートである。

【００４６】まず、ステップＳ１において、ＣＰＵ１３は、第１レジスタ１１３に半導体記憶装置１の全試験領域を試験する入力信号を発生するのに必要なデータを設定すると同時に、第２レジスタ１１４に全試験領域の一部である所定の第１試験領域を試験する入力信号を発生するのに必要なデータを設定する。第１試験領域としては、試験される半導体装置の概略的な特性を示す領域で最小限の領域を設定すればよい。図３に第１試験領域の一例を示す。図３に示すように、たとえば、半導体記憶装置１の記憶容量が６４Ｍｂｉｔであるとしたとき、斜線で示した下位アドレスの１Ｋｂｉｔの部分を第１試験領域として使用することができる。したがって、第１レジスタ１１３には、６４Ｍｂｉｔのすべての記録領域にアクセスする値を設定し、第２レジスタ１１４には下位アドレスの１Ｋｂｉｔの部分のみをアクセスする値を設

定すればよい。

【００４７】次に、ステップＳ２において第１試験領域に対する試験を実行する。ＣＰＵ１３は、切換スイッチ１１５へ第２レジスタ１１４側を接続するように指令し、第２レジスタ１１４から所定のデータが演算器１１２へ出力される。演算器１１２は演算したアドレスデータを出力回路１１１を介して半導体記憶装置１へ出力する。また、同時にセルデータ等の試験用データも半導体記憶装置１へ入力される。半導体記憶装置１は記憶したセルデータを再び読出し、入力回路１２１を介して良否判定回路１２２へ読出したセルデータを出力する。良否判定回路１２２は演算器１１２から出力されるセルデータの期待値データと読出されたセルデータとを比較し特性の良否を判定する。

【００４８】次に、ステップＳ３において、良否判定回路１２２は良否の判定結果を判定結果記憶メモリ１４へ出力する。判定結果記憶メモリ１４は入力された判定結果をシュムプロット図と対応させたマトリックス状の位置と対応させて記憶する。

【００４９】次に、ステップＳ４において、ＣＰＵ１３は、第１試験領域に対するすべての試験条件の試験が終了したか否かを確認する。試験が終了していなければ、ステップＳ１１に移行し、次の試験条件に変更した後、ステップＳ２へ移行し、再び試験を実行する。試験が終了していれば、ステップＳ５へ移行する。上記の処理を行なうことにより、半導体記憶装置１の概略の特性を比較的短時間に試験することが可能となる。ここでは、第１試験領域として全試験領域の６４分の１の試験領域を試験しているので、試験時間は、全試験領域の試験時間の６４分の１となる。

【００５０】次に、ステップＳ５において、ＣＰＵ１３は、判定結果記憶メモリ１４に記憶された良否判定結果を基に特性が良または不良に変化する良／不良の境界点となる試験条件を検索する。図４に第１試験領域の試験結果の一例を示すシュムプロット図を示す。図４に示すように、“不良”（空白）から“良”（“＊”）へ変化する各境界点の試験条件がマトリックス上の位置と対応させられてＣＰＵ１３の内部にある主記憶装置（図示省略）内に蓄えられる。たとえば、境界点Ｐ１はマトリックス状の位置で言えば、縦軸の１番目でかつ横軸の４番目ということになる。これらの境界点に関するデータは、主記憶装置内に記憶されているので、高速にアクセスすることが可能である。また、図４では、境界が１つである場合のシュムプロット図を示しているが、複数の境界がある場合でも、すべての試験条件に対して試験を実行しているので、すべての境界を正確に検出することが可能である。以上の処理により、全試験領域の一部である第１試験領域における完全な良／不良の境界点に関するデータを検出することが可能となる。

【００５１】次に、ステップＳ６において、試験領域を

全試験領域に切換える。ＣＰＵ１３は、入力信号発生回路１１へ試験領域を第１試験領域から全試験領域へ切換えるよう指令をする。入力信号発生回路１１では、切換スイッチ１１５が第２レジスタ１１４から第１レジスタ１１３へ接続を切換える。この結果、演算器１１２から出力されるアドレスデータは全試験領域に対応したアドレスデータとなる。

【００５２】次に、ステップＳ７において、ＣＰＵ１３は、縦軸の試験条件として初期値を設定する。

【００５３】次に、ステップＳ８において、ＣＰＵ１３は境界点付近のみ測定するサブルーチンを実行する。

【００５４】境界点付近のみ測定するサブルーチンについて以下に説明する。半導体記憶装置１の特性により、ステップＳ５で求めた特性の良／不良の境界点は試験領域により多少異なることが考えられる。したがって、全試験領域における試験条件は求めた良／不良の境界点の前後数ポイントの試験条件に対して試験を行なうことにより、全試験領域に対する良／不良の境界点を検出し正確な良否判定結果を得ることができる。境界点を挟む前後の試験条件の幅は試験される半導体装置の特性のばらつきを考慮して決定され、ここでは、一般の半導体記憶装置を考慮し、正確な良否判定結果が得られ、かつ、試験条件の数の少ない値として境界点の前後３ポイントの試験条件に対して試験を行なうものとする。

【００５５】図５は、本実施例による試験順序を説明する図である。図５に示すように、境界点を中心として、左側へ３ポイント進んだ点を試験条件Ｌとし、右側へ３ポイント進んだ点を試験条件Ｒとする。試験条件Ｌから試験条件Ｒまでの間に、境界点が１つだけ存在する場合は良否判定結果として“不良”と判定された側から境界点側へ順次所定の試験条件で試験を行なう。良否判定の試験は、試験領域内に１つでも不良のセルが発見されれば、その時点で試験を中止し、その試験条件に対する試験結果を“不良”として判定するので、全試験領域に対して“良”の結果が出た場合に初めて試験結果として“良”と判定する“良”の場合より“不良”の場合の方が１つの試験条件に対する試験時間を大幅に短縮することが可能だからである。

【００５６】また、試験条件Ｌから試験条件Ｒの間に他の境界点が存在する場合は、その境界点を含まないように試験条件Ｌまたは試験条件Ｒを設定し、良否判定結果として“良”の結果が得られている側から試験を開始するものとする。

【００５７】以下、境界点付近のみ測定のサブルーチンの実際の処理について説明する。まず、ステップＳ１３において、ＣＰＵ１３は自己の主記憶装置内に蓄えられている良／不良の境界点に関する情報をアクセスし、最初の境界点を特定した後その境界点から３ポイント戻ったところの試験条件を試験条件Ｌとして設定する。

【００５８】次に、ステップＳ１４において、ＣＰＵ１

３は試験条件Ｌと境界点の間に他の境界点を含むか否かを確認する。他の境界点を含まない場合はステップＳ１８へ移行する。他の境界点を含む場合は試験条件を変更するためステップＳ１５へ移行する。

【００５９】次に、ステップＳ１５において、ＣＰＵ１３は境界点から３ポイント進んだ点の試験条件を試験条件Ｒとして設定する。

【００６０】次に、ステップＳ１６において、ＣＰＵ１３は試験条件Ｒと境界点の間に他の境界点を含むか否かを確認する。他の境界点を含まない場合はステップＳ１８へ移行する。他の境界点を含む場合は試験条件を変更するためステップＳ１７へ移行する。

【００６１】次に、ステップＳ１７において、ＣＰＵ１３は試験条件Ｌから試験条件Ｒの間に他の境界点を含まないように試験条件Ｌおよび試験条件Ｒを変更する。この結果、試験条件Ｌから試験条件Ｒまでの間には必ず１つの境界点が存在することとなる。

【００６２】次に、ステップＳ１８において、設定された試験条件Ｌから試験条件Ｒの間から前記のような規則に従い開始する試験条件を設定し、その試験条件から試験を実行し、境界点を見つける。

【００６３】次に、ステップＳ１９において、ＣＰＵ１３はすべての境界点が見つかったか否かを確認する。すべての境界点が見つかった場合はこれ以上の試験を継続する必要はないのでサブルーチンによる処理を終了しステップＳ９へ移行する。すべての境界点が見つかっていない場合は、引続き試験を行ない境界点を見つける必要があるので、ステップＳ２０へ移行する。

【００６４】次に、ステップＳ２０において、ＣＰＵ１３は横軸の試験条件を次の境界点を含む試験条件に変更し、ステップＳ１３へ戻り次の境界点を見つけるため以降の処理を継続する。

【００６５】上記の境界点付近のみ測定するサブルーチンの処理が終了した後、ステップＳ９において、ＣＰＵ１３は表示装置または印刷装置（図示省略）に試験結果をシュムプロットとして表示する。

【００６６】次にステップＳ１０において、ＣＰＵ１３は縦軸のすべての試験条件に対して試験が終了したか否かを確認する。縦軸のすべての試験条件に対して試験が終了していれば、処理を終了し、縦軸のすべての試験条件に対して試験が終了していなければステップＳ１２へ移行する。

【００６７】次に、ステップＳ１２において、ＣＰＵ１３は縦軸の試験条件を１ポイント変更し、ステップＳ８へ移行し、以降の処理を継続する。

【００６８】以上の動作により、試験領域の一部である第１試験領域において採取した良／不良の境界点に関する情報を基に、境界点付近の試験条件を設定し、その試験条件のみで全試験領域に対して試験を実行することができ、試験時間を大幅に短縮することが可能となる。また、境界点に関する情報は、すべての試験条件に対して試験をした結果を基に作成されているので、境界点を複数含む特性を有する半導体記憶装置においても、正確にその特性を把握することができる。したがって、半導体装置の特性にかかわらず、高速かつ正確に半導体装置の特性の良否を試験することが可能となる。

【００６９】図６に、本装置により得られたシュムプロット図を示す。図６において、判定結果の良／不良の境界点は“＊”で示されている。図６から明らかなように、本装置によるシュムプロット図は、複数の境界点に対して正確にすべての境界点を検出していることがわかる。また、図７に、実際に試験を行なったポイントを示す図を示す。図７において、“Ｆ”は“不良”、“Ｐ”は“良”、“＊”は境界点をそれぞれ示している。図７から明らかなように、数ポイントの試験条件に対して試験を行なうことにより、１つの境界点を採取することが可能となり、必要な試験条件の数を大幅に低減することが可能となっている。

【００７０】図８に半導体記憶装置のデバイス容量とシュムプロットの採取時間との関係を示す。図８において、実線は本実施例のテスタ、破線はバイナリサーチ手法による従来のテスタ、一点鎖線は従来のテスタをそれぞれ示している。図８から明らかなように、本実施例では、従来のテスタに比べ、約８分の１の時間でシュムプロットを採取することが可能となっている。また、バイナリサーチ手法と比べてほぼ同等の時間で実現されており、バイナリサーチ手法と同等の採取時間で、バイナリサーチ手法では評価できなかった良／不良の境界点を複数有する半導体装置に対しても正確なシュムプロットを採取することが可能となっている。

【００７１】上記実施例では、縦軸の所定の値に対して、少なくとも１つの境界点が存在することを前提として述べたが、境界点が存在しない場合は、横軸の第１パラメータの両極値のみを試験し、判定結果が第１試験領域により得られた判定結果と異なる場合は、新たな境界点を発見するまで、試験を行なうようにすれば、境界点を含まない試験条件に対しても適用することが可能となる。

【００７２】また、上記実施例では、判定結果記憶メモリ１４を設けて判定結果を記憶させたが、ＣＰＵ１３内の主記憶装置あるいは他の記憶装置に記憶させても同様の効果を得ることができる。また、上記実施例では、判定結果記憶メモリ１４内のデータから検索した境界点に関する情報をＣＰＵ１３内の主記憶装置内に記憶するようにしたが、判定結果記憶メモリ１４内に空き領域があればその領域に格納しても同様の効果が得られるし、あるいは、判定結果記憶メモリ１４のデータを消去した後、境界点に関する情報を格納するようにしてもよい。

【００７３】また、上記実施例では、第２レジスタ１１４内に所定の第１試験領域に関するデータを蓄えたが、

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第２レジスタ１１４を設けず、第１レジスタ１１３内に蓄えられている全試験領域に関するデータを基に、たとえば、ダイアゴナルパターン等を用いることにより、半導体記憶装置１内のメモリセルをアクセスするシーケンスを工夫しても特性を比較的短時間に判定することが可能となる。図９はダイアゴナルパターンを示す図である。この場合、図９に示す斜線のメモリセルが第１記録領域として試験を行なうメモリセルとなる。このようなダイアゴナルパターンは、測定される半導体装置の特性が全試験領域に対して均一でなく、所定の局所部分の試験結果では、全試験領域の特性を表わすことができない場合に特に有効である。

【００７４】

【発明の効果】本発明の半導体装置の試験装置においては、第１試験手段により得られた特性の良否結果を基に、試験条件の数が少なく、特性の良否が変化する試験条件を含んだ試験条件で、全試験領域に対する試験を行なうので、複数の試験条件すべてに対して試験を行なうより試験時間を大幅に短縮することが可能となる。また、第１試験手段はすべての試験条件に対して試験が行なわれているので、特性の良否が複雑に変化する半導体装置でも、その特性を正確に把握することが可能となる。この結果、半導体装置の特性にかかわらず、高速かつ正確に半導体装置の特性の良否を試験することが可能となる。

【図面の簡単な説明】

【図１】本発明の一実施例の半導体装置の試験装置の要部の構成を示すブロック図である。

【図２】本発明の一実施例の半導体装置の試験装置の動作を示すフローチャートである。

【図３】第１試験領域の一例を示す図である。

【図４】第１試験領域の試験結果の一例を示す図である。

【図５】本発明の一実施例の半導体装置の試験装置の試験順序を説明する図である。

【図６】本発明の一実施例の半導体装置の試験装置により得られた良否結果を示す図である。

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【図７】本発明の一実施例の半導体装置の試験装置により実際に試験を行なったポイントを示す図である。

【図８】デバイス容量とシュムプロットの採取時間との関係を示す図である。

【図９】ダイアゴナルパターンを示す図である。

【図１０】従来の半導体装置の試験装置の要部の構成を示すブロック図である。

【図１１】シュムプロットの一例を示す図である。

【図１２】従来の半導体装置の試験装置による試験順序を説明する図である。

【図１３】従来の半導体装置の試験装置の動作を示すフローチャートである。

【図１４】従来の半導体装置の試験装置を用いたバイナリサーチ手法による試験順序を説明する図である。

【図１５】従来の半導体装置の試験装置を用いたバイナリサーチ手法による動作を説明するフローチャートである。

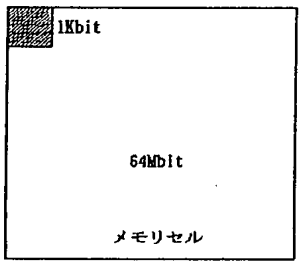
【図１６】良／不良の境界が複数ある半導体装置を試験した場合の良否判定結果を示す図である。

【図１７】図１６に示す特性を有する半導体装置をバイナリサーチ手法により試験した場合の良否判定結果を示す図である。

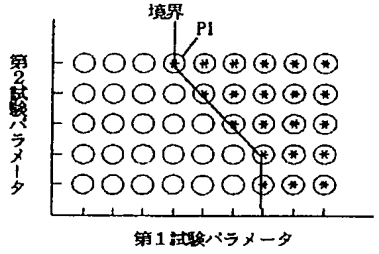
【符号の説明】

１０　テスタ
１１　入力信号発生回路
１２　出力信号発生回路
１３　ＣＰＵ
１４　判定結果記憶メモリ
１１１　出力回路
１１２　演算器
１１３　第１レジスタ
１１４　第２レジスタ
１１５　切換スイッチ
１２１　入力回路
１２２　良否判定回路

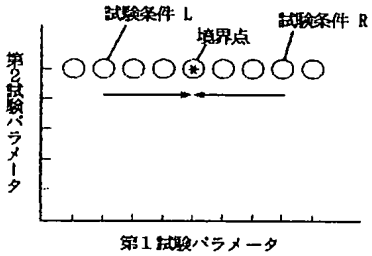
【図３】



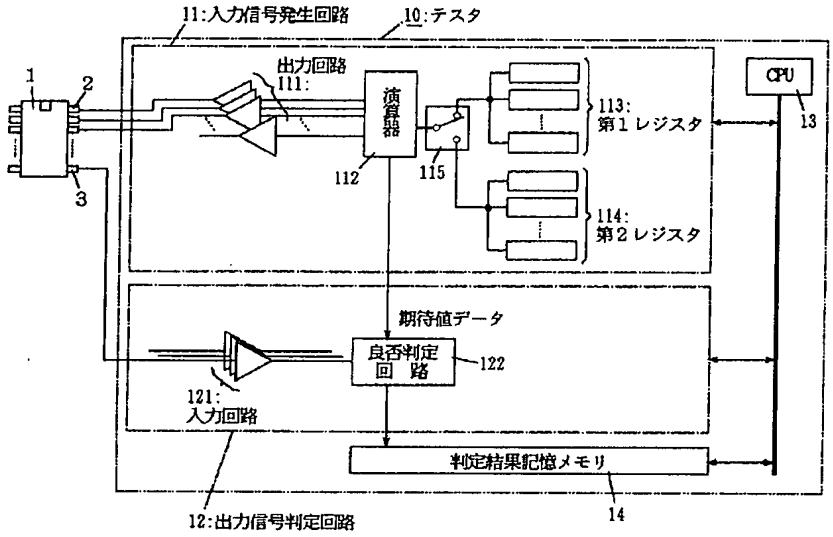
【図４】



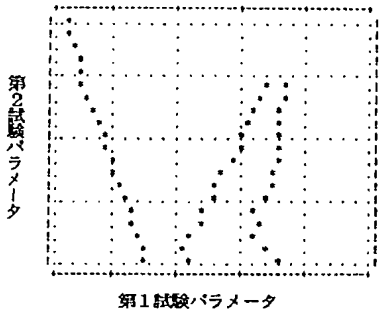
【図５】



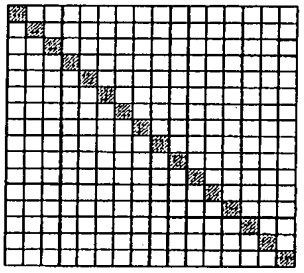
【図１】



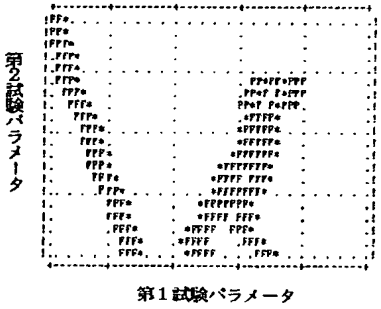
【図６】



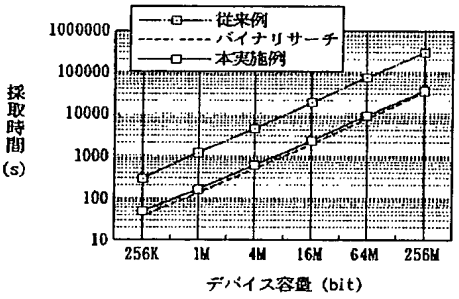
【図９】



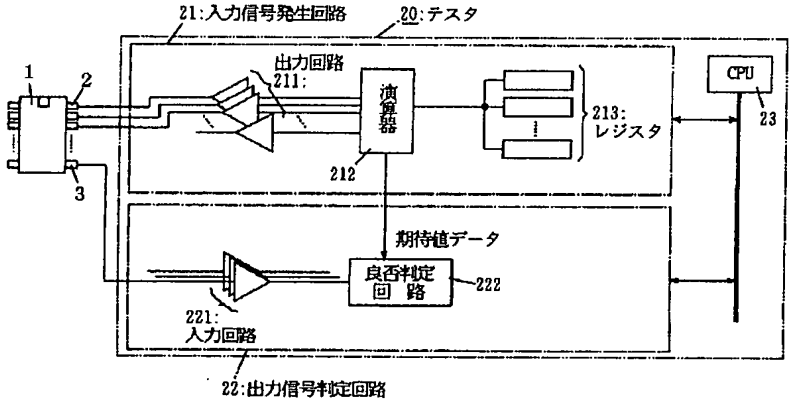
【図７】



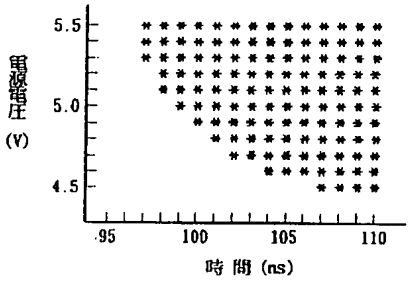
【図８】



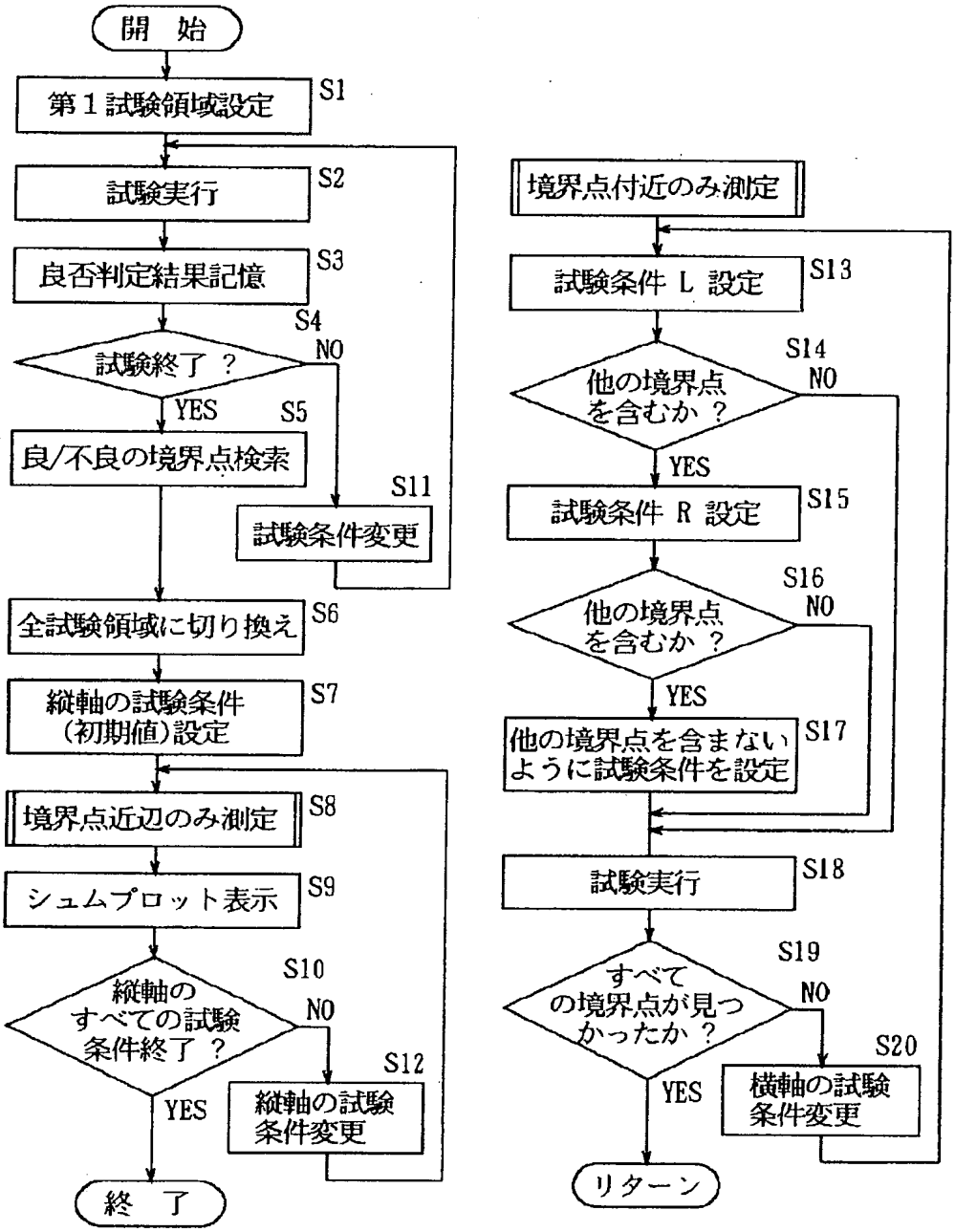
【図１０】



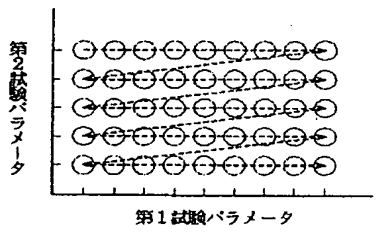
【図１１】



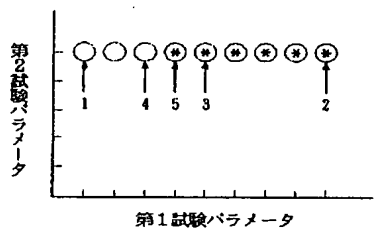
【図２】


開　始
第１試験領域設定
S1
試験実行
S2
良否判定結果記憶
S3
試験終了 ？
S4
NO
YES
S5
良/不良の境界点検索
試験条件変更
S11
全試験領域に切り換え
S6
縦軸の試験条件
(初期値)設定
S7
境界点近辺のみ測定
S8
シュムプロット表示
S9
縦軸の
すべての試験
条件終了 ？
S10
NO
YES
縦軸の試験
条件変更
S12
終　了
境界点付近のみ測定
試験条件 L 設定
S13
他の境界点
を含むか ？
S14
NO
YES
試験条件 R 設定
S15
他の境界点
を含むか ？
S16
NO
YES
他の境界点を含まない
ように試験条件を設定
S17
試験実行
S18
すべて
の境界点が見つ
かったか ？
S19
NO
YES
横軸の試験
条件変更
S20
リターン

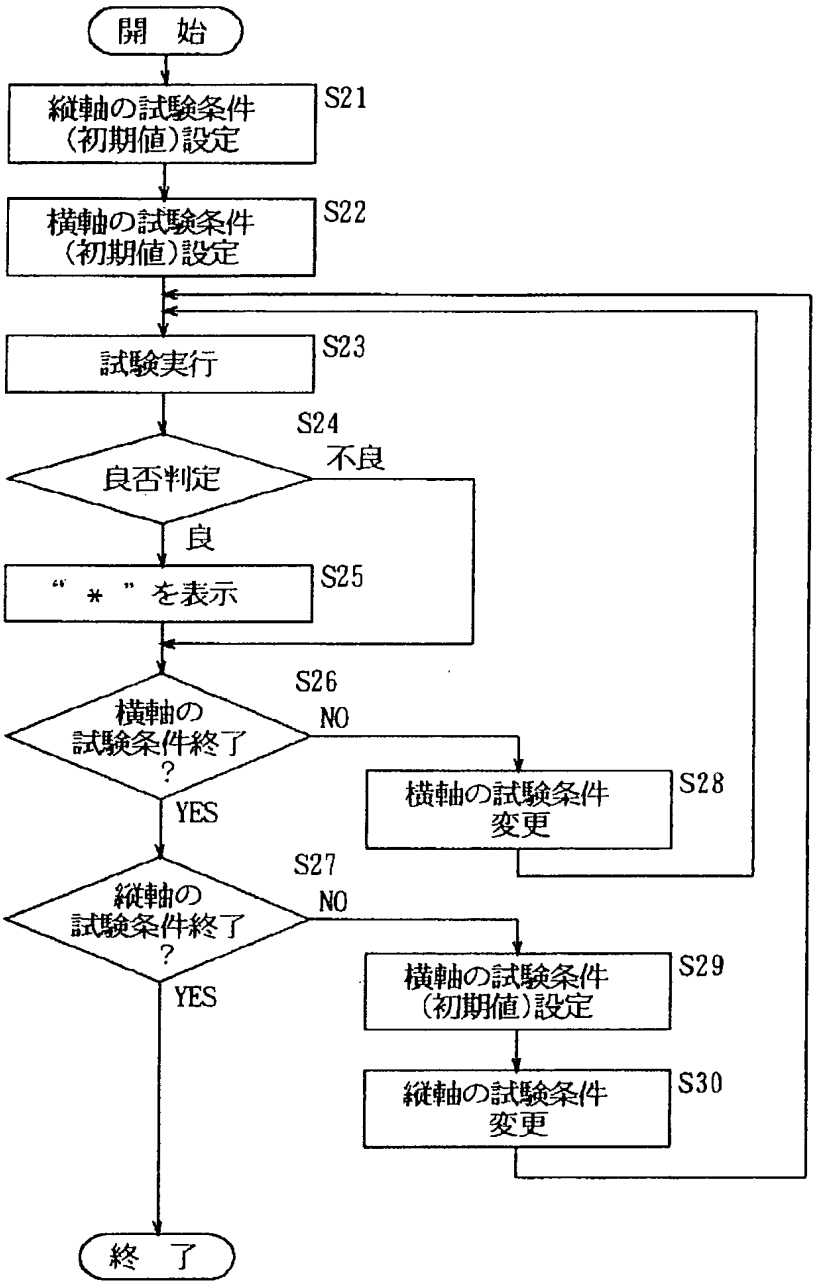
【図１２】


第2試験パラメータ
第1試験パラメータ

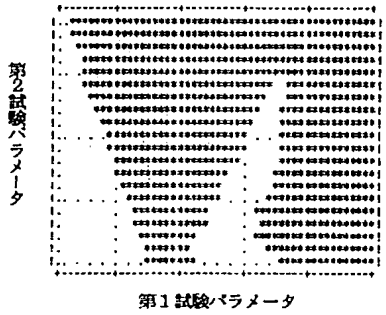
【図１４】


第2試験パラメータ
1
4
5
3
2
第1試験パラメータ

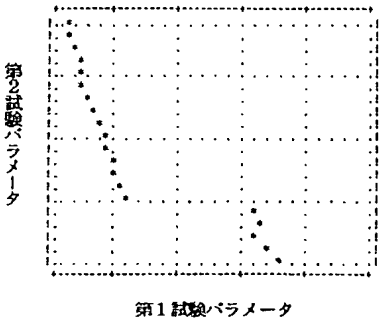
【図１３】


開　始
縦軸の試験条件(初期値)設定
S21
横軸の試験条件(初期値)設定
S22
試験実行
S23
S24
良否判定
不良
良
“ * ”を表示
S25
S26
横軸の試験条件終了？
NO
YES
横軸の試験条件変更
S28
S27
縦軸の試験条件終了？
NO
YES
横軸の試験条件(初期値)設定
S29
縦軸の試験条件変更
S30
終　了

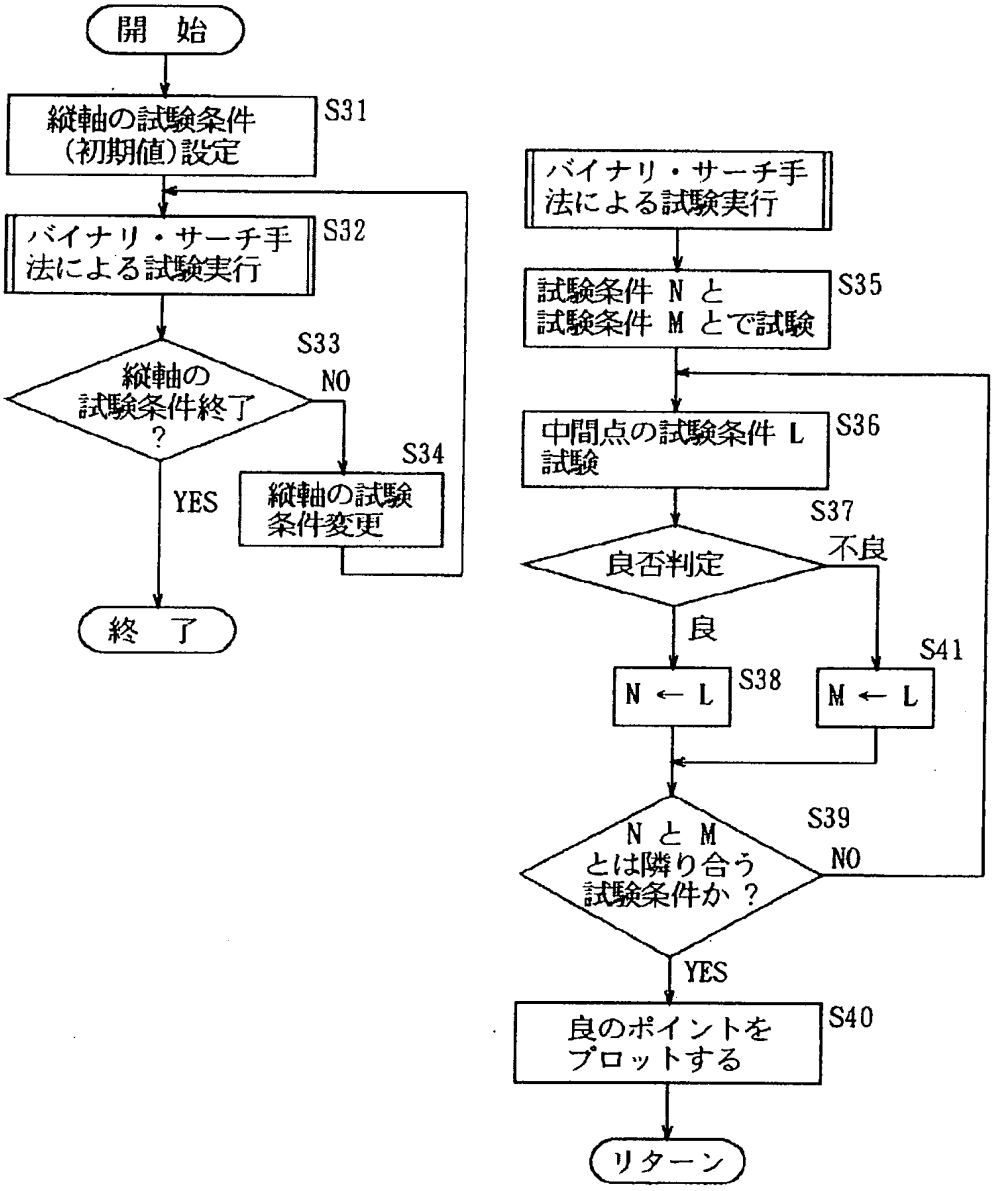
【図１６】


第2試験パラメータ
第1試験パラメータ

【図１７】


第2試験パラメータ
第1試験パラメータ

【図１５】


開　始
縦軸の試験条件
(初期値)設定
S31
バイナリ・サーチ手
法による試験実行
S32
縦軸の
試験条件終了
？
S33
NO
YES
S34
縦軸の試験
条件変更
終　了
バイナリ・サーチ手
法による試験実行
試験条件 N と
試験条件 M とで試験
S35
中間点の試験条件 L
試験
S36
S37
良否判定
不良
良
S41
N ← L
S38
M ← L
N と M
とは隣り合う
試験条件か ？
S39
NO
YES
良のポイントを
プロットする
S40
リターン

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] About the testing device of the semiconductor device which examines about the quality of the property of a semiconductor device over two or more test conditions, especially, this invention changes two or more test conditions continuously, and relates to the testing device of the semiconductor device which creates the SHUMU plot which displays a quality judging result in the shape of a matrix.
[0002]
[Description of the Prior Art] High integration of a semiconductor device is attained by advance of semiconductor technology, for example, the storage capacity of a semiconductor memory is increasing by leaps and bounds in the past several years. If it is going to examine about the quality of the property of all test areas to the semiconductor device which has such a mass storage capacity, test time will also increase by leaps and bounds with increase of storage capacity. Development of the testing device of the semiconductor device which is a short time and judges the quality result of an exact property is strongly desired under such a background.
[0003] Hereafter, it explains, referring to a drawing about the testing device (it abbreviates to a circuit tester below) of the conventional semiconductor device. Drawing 10 is the block diagram showing the configuration of the important section of the conventional circuit tester.
[0004] In drawing 10 , a circuit tester 20 contains the input signal generating circuit 21, the output signal judging circuit 22, and CPU (arithmetic and program control)23. It connects with the input signal generating circuit 21 and the output signal judging circuit 22, and CPU23 controls actuation of each part. By the operating command outputted from CPU23, the input signal generating circuit 21 creates the predetermined data for a trial, and outputs the data for a trial to a semiconductor memory 1 through the signal input pin 2 grade of a semiconductor memory 1. It consists of control data which control each actuation of the store of the address data which specify the address of the memory cell in a semiconductor memory 1, the cell data stored in the memory cell, and a semiconductor memory 1, read-out, etc. as data for a trial. Here, generating circuits without the direct relation to the meaning of this invention, such as a cell data and control data, etc. omit illustration and explanation, and explain them below about address data at a detail.
[0005] The input signal generating circuit 21 contains an output circuit 211, a computing element 212, and a register 213. It connects with a computing element 212, the maximum of the address of data required for creation of address data, for example, all the test areas of a semiconductor memory 1, the minimum value, etc. are memorized beforehand, and a register 213 outputs predetermined data to a computing element 212 according to the operating command from CPU23. It connects with an output circuit 211, and a computing element 212 creates predetermined address data based on the data outputted from the register 213, and outputs them to an output circuit 211. It connects with the signal input pin 2 of a semiconductor memory 1, and an output circuit 211 inputs the inputted address data into a semiconductor memory 1. A semiconductor memory 1 memorizes the cell data separately transmitted

in the predetermined memory cell based on the inputted address data.

[0006] Next, a semiconductor memory 1 outputs the written-in cell data to the output signal judging circuit 22 through read-out and the signal output pin 3. The output signal judging circuit 22 includes an input circuit 221 and the quality judging circuit 222. The cell data outputted from the semiconductor memory 1 is inputted into the quality judging circuit 222 through an input circuit 221. The quality judging circuit 222 is connected with a computing element 212, and the expected-value data showing the cell data which the input signal generating circuit 21 made memorize are inputted from a computing element 212. The quality judging circuit 222 compares expected-value data with the read cell data, and judges the quality of a property. A judgment result is outputted to CPU23, and based on this judgment result, CPU23 displays a test result on a display or an airline printer (illustration abbreviation), and becomes possible [getting to know about the quality of the property of a semiconductor memory 1].

[0007] Next, the approach of the characteristic test of the semiconductor memory using the circuit tester 20 constituted as mentioned above is explained. One of the characteristic tests of a semiconductor memory has a SHUMU plot. A SHUMU plot examines by two or more test conditions to which two test condition parameters or three test condition parameters were changed at the predetermined spacing among some kinds of test condition parameters (for example, supply voltage, input timing of various signals, etc.), plots the quality judging result in the shape of [of two-dimensional or a three dimension] a matrix, and examines the property of a semiconductor memory.

[0008] An example of a SHUMU plot is shown in drawing 11 . The time amount which performs the quality judging of the data outputted as a test condition parameter from the supply voltage and the semiconductor memory which are given to a semiconductor memory is used. In drawing 11 , the time amount which performs the quality judging of the data which the supply voltage of 11 points is changed to 0.1V unit to 5.5V-4.5V for an axis of ordinate, and are outputted in supply voltage is changing the test condition of 16 points to the unit for 1ns for an axis of abscissa from 95ns till 110ns. Consequently, 11 points x 16 points = a trial is carried out by each test condition of 176 points, if a test result is "good", "*" will be displayed on that point, and if "poor", it is leaving in the null. By displaying as a SHUMU plot shown in drawing 11 , it becomes possible to recognize the quality of the test result to two or more test conditions at a glance.

[0009] Next, in order to create the above-mentioned SHUMU plot, the sequence of carrying out each test condition is explained. Drawing 12 is drawing showing the sequence of carrying out each test condition. As shown in drawing 12 , each test condition is carried out in sequence as an arrow head shows. First, after examining changing the 1st trial parameter of an axis of abscissa at the predetermined spacing after fixing the conditions of the 2nd trial parameter of an axis of ordinate and completing a trial to all the test conditions of an axis of abscissa, the test condition of the 2nd trial parameter of an axis of ordinate is changed at the predetermined spacing, and it examines similarly, and it repeats until a trial is completed about all test conditions.

[0010] Next, actuation of the conventional circuit tester which creates the SHUMU plot shown in drawing 12 is explained below. Drawing 13 is a flow chart explaining actuation of the conventional circuit tester. The flow chart shown in drawing 13 is beforehand memorized as a program by the storage in CPU23, and when CPU23 performs the program if needed, it is realized.

[0011] First, in step S21, CPU23 sets up the initial value of the test condition of an axis of ordinate.

[0012] Next, in step S22, CPU23 sets up the initial value of the test condition of an axis of abscissa.

[0013] Next, in step S23, the input signal generating circuit 21 and the output signal judging circuit 22 are ordered CPU23 so that it may examine by the set-up test condition, and it performs a trial.

[0014] Next, in step S24, the output signal judging circuit 22 judges the quality of a test result, and outputs a judgment result to CPU23. Based on the inputted quality judging result, CPU23 will shift to step S25, if a test result is "good", and if "poor", it will shift to step S26.

[0015] Next, it sets to step S25 and CPU23 displays "*" on the location which shows the predetermined test condition of a SHUMU plot. Since step S25 is skipped on the other hand when judged with it being "poor", nothing is displayed on a SHUMU plot.

[0016] Next, in step S26, it checks whether the trial has ended CPU23 to all the test conditions of an

axis of abscissa. If the trial is not completed, in order to set up the test condition of the following axis of abscissa, it shifts to step S28. If the trial is completed, in order to set up the test condition of the following axis of ordinate, it shifts to step S27.

[0017] Next, in step S26, when it is judged that the test condition of an axis of abscissa is not completed and it shifts to step S28, CPU23 changes the test condition of an axis of abscissa into the following test condition, shifts to step S23, and repeats subsequent processings.

[0018] On the other hand, when it is judged that it ended about all the test conditions of an axis of abscissa in step S26, in step S27, it checks whether the trial to all the test conditions of an axis of ordinate has ended CPU23. If the test condition of an axis of ordinate is not completed, and it carried out after that to step S29 and has ended to it in order to set up the following test condition, since the trial to all test conditions is completed, processing will be ended.

[0019] Next, when it is judged that the test condition of an axis of ordinate is not completed in step S27 and it shifts to step S29, CPU23 sets up initial value as a test condition of an axis of abscissa.

[0020] Next, in step S30, CPU23 changes the test condition of an axis of ordinate into the following test condition, shifts to step S23, and continues subsequent processings.

[0021] By the above actuation, a circuit tester 20 carries out the trial to all test conditions in the sequence of the test condition shown in drawing 12 , and becomes possible [creating the SHUMU plot showing the quality judging result of each test condition].

[0022] Next, the trial to all test conditions is performed as mentioned above, and a SHUMU plot is not created, but by examining in predetermined sequence explains below creation of the SHUMU plot by the binary search technique which can shorten test time. Drawing 14 is drawing explaining the test procedure by the binary search technique which used the conventional circuit tester.

[0023] As shown in drawing 14 , the 1st trial parameter is taken along an axis of abscissa, and the 2nd trial parameter is taken along an axis of ordinate. First, after fixing the 2nd trial parameter of an axis of ordinate to predetermined conditions, it examines by the test condition at the left end of the 1st trial parameter of an axis of abscissa. Next, it examines to the same 2nd trial parameter by the test condition at the right end of the 1st trial parameter of an axis of abscissa. The result of the test condition shown by the arrow head 2 serves as "good" ("*"), and that the result of the test condition shown by the test result and the arrow head 1 is "poor" (null), and when both test judging results differ, both middle point is examined. Here, the next trial is performed as a middle test condition by the test condition shown by the arrow head 3. When a test result is "good" at this time, the next trial is performed by the test condition between the test condition shown by the arrow head 1, and the test condition shown by the arrow head 3, for example, the conditions shown by the arrow head 4. When the test result in the test condition shown in an arrow head 4 is "poor", the next trial is performed by the test condition shown by the arrow head 5 which it is between the test condition shown by the arrow head 4, and the test condition shown by the arrow head 3. Since between the test condition shown by the arrow head 4 and the test conditions shown by the arrow head 5 serves as the boundary point of good/defect when the test result of the test condition shown by the arrow head 5 is "good", "*" is plotted into the part of the test condition shown by the arrow head 5.

[0024] Since the boundary point of good/defect can be specified without examining to all test conditions by examining by the test condition in the meantime when the binary search technique examines by two different test conditions as stated above, and test results differ, it becomes possible to shorten test time. For example, to nine test conditions, by examining by five test conditions, the boundary point of good/defect can be specified and test time is shortened by 5/9 in drawing 14 . By examining the above-mentioned processing to each test condition of the 2nd trial parameter, the whole test time can be shortened similarly and it becomes possible to create a SHUMU plot at a high speed.

[0025] Next, actuation of the conventional circuit tester by the above-mentioned binary search technique is explained. Drawing 15 is a flow chart explaining actuation of the conventional circuit tester by the binary search technique.

[0026] First, in step S31, CPU23 sets up initial value as a test condition of an axis of ordinate.

[0027] Next, in step S32, CPU23 performs the subroutine which performs test activation by the binary

search technique. The subroutine of the test activation by the binary search technique is processed as follows.

[0028] First, in step S35, it examines by the test condition N which shows "good" as a quality judging result, and the test condition M which shows a "defect."

[0029] Next, in step S36, it examines by the test condition L of the midpoint of a test condition N and a test condition M.

[0030] Next, in step S37, the quality judging in the test condition L of a midpoint is performed. When a judgment result is "poor", it shifts to step S41, and in the case of "good", it shifts to step S38.

[0031] When judged with "good" at step S37, in step S38, a test condition N is transposed to a test condition L.

[0032] On the other hand, in step S37, when it is judged that it is "poor", in step S41, a test condition M is transposed to a test condition L.

[0033] By the above processing, the boundary point of good/defect will exist between a test condition N and a test condition M.

[0034] Next, in step S39, it checks whether a test condition N and a test condition M are ****** test conditions. Since the boundary point of good/defect can be specified when it is a ****** test condition, it shifts to step S40. If it is not a ****** test condition, since the boundary point of good/defect may exist between a test condition N and a test condition M, it will shift to step S36 and will examine again about the test condition L of a midpoint.

[0035] Next, in step S40, the point of "good" used as the boundary point of good/defect is plotted. Without examining to all test conditions, the test condition used as the boundary point of good/defect can be specified, and the above processing enables it to create a SHUMU plot at a high speed.

[0036]

[Problem(s) to be Solved by the Invention] Since the conventional circuit tester is constituted as mentioned above, in order to extract a SHUMU plot as a characteristic test, the trial needed to be repeated to all the test conditions set as the axis of ordinate and the axis of abscissa, and there was a trouble that test time became very long. For example, supposing it examined all test areas by the predetermined test condition in the case of the semiconductor memory of 16Mbit, about 4.6 hours was required and very huge time amount was needed. Moreover, this test time increases by leaps and bounds with the increment in the capacity of a semiconductor memory, and becoming a problem bigger future still is expected.

[0037] Moreover, in the binary search technique currently developed as an approach of shortening test time, there was a trouble that it could not be used to the semiconductor device in which the property that the boundary point of good/defect exists more than plurality is shown. The SHUMU plot at the time of examining the semiconductor memory which has two or more boundaries of good ("*")/defect (null) in drawing 16 is shown. As shown in drawing 16 , when there are two or more boundaries of good/defect, in order to detect only one boundary, other boundaries will be disregarded by the binary search technique. The SHUMU plot at the time of examining the semiconductor memory which has the property shown in drawing 17 at drawing 16 by the binary search technique is shown. Since, as for the boundary of good/defect, only one was detected and the other boundary points were not detected so that clearly from drawing 17 , the quality judging result in which it completely made a mistake was displayed, and there was a problem that exact evaluation was unrealizable.

[0038] This invention is for solving the above-mentioned technical problem, and it aims at offering a high speed and the testing device of a semiconductor device which can examine the quality of the property of a semiconductor device correctly irrespective of the property of a semiconductor device.

[0039]

[Means for Solving the Problem] In the 1st test area whose testing devices of the semiconductor device of this invention are a part of all test areas of a semiconductor device A 1st trial means to examine about the quality of the property of a semiconductor device over two or more test conditions, In a decision means to determine the 2nd test condition which is a part of two or more test conditions based on the quality result of the property acquired by the 1st trial means including the 1st test condition from which

the quality of a property changes at least, and all the test areas of a semiconductor device A 2nd trial means to examine about the quality of the property of a semiconductor device over the 2nd test condition determined by the decision means is included.

[0040]

[Function] In the testing device of the semiconductor device of this invention, since it examines about the quality of the property of a semiconductor device to two or more test conditions of all in the 1st test area which is a part of all test areas, a perfect quality test result can be obtained. Since the 2nd test condition which is a part of two or more test conditions is determined based on this test result including the 1st test condition from which the quality of a property changes, the 2nd test condition has few those numbers than all test conditions, and turns into a test condition including the test condition from which the quality of a property surely changes. All test areas are examined about the quality of the property of a semiconductor device over this 2nd test condition.

[0041]

[Example] It explains referring to a drawing hereafter about the testing device (a circuit tester is called below like the conventional example) of the semiconductor device which is one example of this invention. Drawing 1 is the block diagram showing the configuration of the important section of the circuit tester of one example of this invention.

[0042] In drawing 1 , a circuit tester 10 contains the input signal generating circuit 11, the output signal judging circuit 12, CPU (arithmetic and program control)13, and the judgment result storage memory 14. It connects with the input signal generating circuit 11, the output signal judging circuit 12, and the judgment result storage memory 14, respectively, and CPU13 controls actuation of each part. The input signal generating circuit 11 answers the command signal of operation outputted from CPU13, creates the data for a trial, and inputs them into a semiconductor memory 1 through the input signal pin 2. As data for a trial, it consists of cell datas stored in the address data and the predetermined memory cell which specify the address of the memory cell in a semiconductor memory 1 as usual. Although a cell data etc. is inputted into a semiconductor memory 1 like the conventional circuit tester, since the meaning of this invention does not have direct relation, the generating circuit of a cell data etc. omits the explanation while omitting illustration.

[0043] A semiconductor memory 1 outputs the cell data memorized based on the data for a trial outputted from the input signal generating circuit 11 to the output signal judging circuit 12 through read-out and the signal output pin 3. The output-signal judging circuit 12 compares the inputted cell data with the expected-value data outputted from the input signal generating circuit 11, and outputs the judgment result of a quality to the judgment result storage memory 14 and CPU13. The judgment result storage memory 14 memorizes the judgment result of the quality outputted from the output signal judging circuit 12, and outputs it to CPU13 if needed.

[0044] The input signal generating circuit 11 contains an output circuit 111, a computing element 112, the 1st register 113, the 2nd register 114, and a change-over switch 115. The 1st register 113 is storing data required to generate the input signal for examining all the memory space of a semiconductor memory 1. For example, they are the maximum of the address corresponding to all the test areas of a semiconductor memory 1, the minimum value, etc. The 2nd register 114 is storing data required to generate the input signal for examining a part of memory capacity of a semiconductor memory 1. For example, they are the maximum of the address corresponding to the predetermined field of a test area, the minimum value, etc. A change-over switch 115 switches connection between the 1st register 113 and the 2nd register 114, and a computing element 112. That is, when examining all the test areas of a semiconductor memory 1, the 1st register 113 is specified and the data corresponding to all test areas are outputted to a computing element 112. Moreover, when examining a part of test area, the 2nd register 114 is connected, and the data corresponding to a predetermined test area are outputted to a computing element 112. A computing element 112 creates predetermined address data based on the data inputted from the 1st register 113 or the 2nd register 114, and outputs them to an output circuit 111. After an output circuit 111 operates the inputted address data orthopedically to a predetermined wave, it is outputted to a semiconductor memory 1 through the signal input pin 2. Data for a trial other than the

above-mentioned address data are created like the conventional circuit tester, and are inputted into a semiconductor memory 1. The output signal judging circuit 12 includes an input circuit 121 and the quality judging circuit 122. The semiconductor memory 1 which memorized the outputted cell data outputs the memorized cell data to an input circuit 121 through read-out and the signal output pin 3 again from the input signal generating circuit 11. The read cell data is outputted to the quality judging circuit 122 through an input circuit 121. The expected-value data in which the cell data memorized from the computing element 112 is shown are outputted to the quality judging circuit 122, this expected-value data is compared with the inputted cell data, and the quality of a property is judged. The quality judging circuit 122 outputs a judgment result to CPU13, when the judgment result of a quality is a thing to all test areas, and when it is a part of test area, it outputs a judgment result to the judgment result storage memory 14. The judgment result storage memory 14 memorizes the judgment result of some qualities of a test area, and CPU13 discriminates the boundary point of good/defect from which a property changes to good or a defect from the memorized judgment result. Based on the identified boundary point, CPU13 sets up a predetermined test condition including the test condition from which the quality of a property changes, and it orders it it so that all test areas may be examined by the test condition to the input signal generating circuit 11.

[0045] Next, actuation of the circuit tester constituted as mentioned above is explained to a detail. Drawing 2 is a flow chart explaining actuation of a circuit tester.

[0046] First, in step S1, CPU13 sets up data required to generate the input signal which examines the 1st predetermined test area which is a part of all test areas to the 2nd register 114 at the same time it sets up data required to generate the input signal which examines all the test areas of a semiconductor memory 1 to the 1st register 113. What is necessary is just to set up the minimum field in the field which shows the rough property of the semiconductor device examined as the 1st test area. An example of the 1st test area is shown in drawing 3 . As shown in drawing 3 , for example, when the storage capacity of a semiconductor memory 1 is 64Mbit, the part of 1Kbit of the lower address shown with the slash can be used as the 1st test area. Therefore, what is necessary is to set the value which accesses all the record sections of 64Mbit to the 1st register 113, and just to set the value which accesses only the part of 1Kbit of a lower address to the 2nd register 114.

[0047] Next, the trial to the 1st test area is performed in step S2. It is ordered CPU13 so that the 2nd register 114 side may be connected to a change-over switch 115, and predetermined data are outputted to a computing element 112 from the 2nd register 114. A computing element 112 outputs the calculated address data to a semiconductor memory 1 through an output circuit 111. Moreover, data for a trial, such as a cell data, are also inputted into a semiconductor memory 1 at coincidence. A semiconductor memory 1 outputs the cell data which read the memorized cell data to the quality judging circuit 122 through read-out and an input circuit 121 again. The quality judging circuit 122 compares the expected-value data of the cell data outputted from a computing element 112 with the read cell data, and judges the quality of a property.

[0048] Next, in step S3, the quality judging circuit 122 outputs the judgment result of a quality to the judgment result storage memory 14. The inputted judgment result is made to correspond with a SHUMU plot and the location of the shape of a matrix it was made to correspond, and the judgment result storage memory 14 memorizes it.

[0049] Next, in step S4, it checks whether the trial of all the test conditions over the 1st test area has ended CPU13. If the trial is not completed, after shifting to step S11 and changing into the following test condition, it shifts to step S2 and a trial is performed again. If the trial is completed, it will shift to step S5. By performing the above-mentioned processing, it becomes possible to examine the property of the outline of a semiconductor memory 1 comparatively for a short time. Here, since 1/64 of the test areas of all test areas are examined as the 1st test area, test time drops to 1/64 of the test time of all test areas.

[0050] Next, in step S5, CPU13 searches the test condition from which a property serves as the boundary point of good/defect which changes to good or a defect based on the quality judging result memorized by the judgment result storage memory 14. The SHUMU plot showing an example of the test result of the 1st test area in drawing 4 is shown. As shown in drawing 4 , it is stored in the main

storage (illustration abbreviation) which is made to correspond to the test condition of each boundary point which changes from it being "poor" (null) to "good" ("*") with the location on a matrix, and has it in the interior of CPU13. For example, if it says in a matrix-like location, the boundary point P1 is the 1st of an axis of ordinate, and will call it the 4th of an axis of abscissa. Since the data about these boundary points are memorized in main storage, they can access a high speed. Moreover, although drawing 4 shows the SHUMU plot in case the number of boundaries is one, since the trial is performed to all test conditions even when there are two or more boundaries, it is possible to detect all boundaries correctly. The above processing enables it to detect the data about the boundary point of perfect good/defect in the 1st test area which is a part of all test areas.

[0051] Next, in step S6, a test area is switched to all test areas. CPU13 orders so that a test area may be switched to the input signal generating circuit 11 from the 1st test area to all test areas. In the input signal generating circuit 11, a change-over switch 115 switches connection to the 1st register 113 from the 2nd register 114. Consequently, the address data outputted from a computing element 112 turn into address data corresponding to all test areas.

[0052] Next, in step S7, CPU13 sets up initial value as a test condition of an axis of ordinate.

[0053] Next, in step S8, CPU13 performs the subroutine which measures near the boundary point.

[0054] The subroutine which measures near the boundary point is explained below. It is possible that the boundary point of the good/defect of the property searched for at step S5 changes somewhat with test areas with the property of a semiconductor memory 1. Therefore, by examining to the test condition of several points before and after the boundary point of the good/defect searched for, the test condition in all test areas can detect the boundary point of good/defect to all test areas, and can obtain an exact quality judging result. The width of face of a test condition before and after inserting the boundary point is determined in consideration of dispersion in the property of the semiconductor device examined, and in consideration of a common semiconductor memory, an exact quality judging result shall be obtained and it shall examine to the test condition of three points here before and after the boundary point as a value with few test conditions.

[0055] Drawing 5 is drawing explaining the test procedure by this example. As shown in drawing 5 , the point which went to left-hand side 3 point focusing on the boundary point is made into a test condition L, and the point which went to right-hand side 3 point is made into a test condition R. When only the one boundary point exists in before the test condition L blank test conditions R, it examines by the predetermined test condition one by one to a boundary point side from the side judged that is "poor" as a quality judging result. If at least one cel of a defect is discovered in a test area, since the trial of a quality judging will stop a trial at the time and will judge the test result to the test condition as "poor" It is because the direction in the case of being "poor"er than the case of the "good" judged as a test result for the first time to be "good" is able to shorten the test time to one test condition sharply when the result of "good" comes out to all test areas.

[0056] Moreover, when other boundary points exist among the test condition L blank test conditions R, a test condition L or a test condition R shall be set up so that the boundary point may not be included, and the side blank test from which the result of "good" is obtained as a quality judging result shall be started.

[0057] Hereafter, actual processing of the subroutine of measurement of near the boundary point is explained. First, in step S13, CPU13 accesses the information about the boundary point of the good/defect currently stored in self main storage, and after it specifies the first boundary point, it sets up the test condition which returned from the boundary point 3 point as a test condition L.

[0058] Next, in step S14, it checks whether CPU13 contains other boundary points between a test condition L and the boundary point. When other boundary points are not included, it shifts to step S18. When other boundary points are included, in order to change a test condition, it shifts to step S15.

[0059] Next, in step S15, CPU13 sets up the test condition of the point which progressed 3 point from the boundary point as a test condition R.

[0060] Next, in step S16, it checks whether CPU13 contains other boundary points between a test condition R and the boundary point. When other boundary points are not included, it shifts to step S18.

When other boundary points are included, in order to change a test condition, it shifts to step S17.
[0061] Next, in step S17, CPU13 changes a test condition L and a test condition R so that other boundary points may not be included among the test condition L blank test conditions R. Consequently, the one boundary point will surely exist in before the test condition L blank test conditions R.
[0062] Next, in step S18, the test condition started according to the above regulations from between the set-up test condition L blank test conditions R is set up, the test condition blank test is performed, and the boundary point is found.
[0063] Next, in step S19, it is checked whether all the boundary points have been found in CPU13. Since it is not necessary to continue the trial beyond this when all the boundary points are found, processing by the subroutine is ended and it shifts to step S9. Since it is necessary to examine succeedingly and to find the boundary point when all the boundary points are not found, it shifts to step S20.
[0064] Next, in step S20, CPU13 changes the test condition of an axis of abscissa into the test condition containing the following boundary point, and in order that it may return to step S13 and may find the following boundary point, it continues subsequent processings.
[0065] After processing of the subroutine which measures near [above] the boundary point is completed, in step S9, CPU13 displays a test result on a display or an airline printer (illustration abbreviation) as a SHUMU plot.
[0066] Next, in step S10, it checks whether the trial has ended CPU13 to all the test conditions of an axis of ordinate. If the trial is completed to all the test conditions of an axis of ordinate, processing is ended and the trial is completed to no test conditions of an axis of ordinate, it will shift to step S12.
[0067] Next, in step S12, CPU13 changes the test condition of an axis of ordinate 1 point, shifts to step S8, and continues subsequent processings.
[0068] Based on the information about the boundary point of the good/defect extracted in the 1st test area which is a part of test area, the test condition near the boundary point can be set up, a trial can be performed to all test areas only by the test condition, and the above actuation enables it to shorten test time sharply. Moreover, since the information about the boundary point is created based on the result of having examined to all test conditions, it can grasp the property correctly also in the semiconductor memory which has a property containing two or more boundary points. Therefore, it becomes possible a high speed and to examine the quality of the property of a semiconductor device correctly irrespective of the property of a semiconductor device.
[0069] The SHUMU plot acquired with this equipment by drawing 6 is shown. In drawing 6 , the boundary point of the good/defect of a judgment result is shown by "*." It turns out that the SHUMU plot by this equipment has detected all the boundary points correctly to two or more boundary points so that clearly from drawing 6 . Moreover, drawing showing the point which actually examined to drawing 7 is shown. In drawing 7 , in "F", a defect and "P" show "good" and "*" shows the boundary point, respectively. It is possible by examining to the test condition of several points to become possible to extract the one boundary point and to reduce the number of required test conditions sharply so that clearly from drawing 7 .
[0070] The relation between the device capacity of a semiconductor memory and the extraction time amount of a SHUMU plot is shown in drawing 8 . In drawing 8 , the conventional circuit tester [according / a broken line / to the binary search technique] according [a continuous line] to the circuit tester of this example and the alternate long and short dash line show the conventional circuit tester, respectively. In this example, it is possible to extract a SHUMU plot by the time amount of about 1/8 compared with the conventional circuit tester so that clearly from drawing 8 . Moreover, compared with the binary search technique, it realizes by almost equivalent time amount, and it is possible to extract an exact SHUMU plot by extraction time amount equivalent to the binary search technique also to the semiconductor device which has two or more boundary points of the good/defect which was not able to be evaluated by the binary search technique.
[0071] Although the above-mentioned example described to the predetermined value of an axis of ordinate on the assumption that at least one boundary point existed When it differs from the judgment

result from which only the two-poles value of the 1st parameter of an axis of abscissa was examined, and the judgment result was obtained by the 1st test area when the boundary point did not exist If it is made to examine until it discovers the new boundary point, it will become possible to apply also to the test condition which does not contain the boundary point.

[0072] Moreover, although the judgment result storage memory 14 was formed and the judgment result was made to memorize in the above-mentioned example, the same effectiveness can be acquired even if it makes the main storage or other storage in CPU13 memorize. Moreover, if a free area is in the judgment result storage memory 14, even if it stores in the field, after acquiring the same effectiveness or eliminating the data of the judgment result storage memory 14, you may make it store the information about the boundary point, although the information about the boundary point searched from the data in the judgment result storage memory 14 was memorized in the main storage in CPU13 in the above-mentioned example.

[0073] Moreover, by not forming the 2nd register 114 but using for example, a diagonal pattern etc. based on the data about all the test areas currently stored in the 1st register 113, although the data about the 1st predetermined test area were stored in the 2nd register 114 in the above-mentioned example, even if it devises the sequence which accesses the memory cell in a semiconductor memory 1, it becomes possible to judge a property comparatively for a short time. Drawing 9 is drawing showing a diagonal pattern. In this case, the memory cell of the slash shown in drawing 9 turns into a memory cell which examines as the 1st record section. Its property of the semiconductor device measured is not uniform to all test areas, and such a diagonal pattern is effective especially when the property of all test areas cannot be expressed with the test result of a predetermined partial part.

[0074]

[Effect of the Invention] It is the test condition which included the test condition from which there are few test conditions and the quality of a property changes based on the quality result of the property acquired by the 1st trial means in the testing device of the semiconductor device of this invention, and since the trial to all test areas is performed, it becomes more possible rather than examining to two or more test conditions of all shortening test time sharply. Moreover, it becomes possible [the 1st trial means] to grasp the property correctly also with the semiconductor device from which the quality of a property changes intricately, since the trial is performed to all test conditions. Consequently, it becomes possible a high speed and to examine the quality of the property of a semiconductor device correctly irrespective of the property of a semiconductor device.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] About the testing device of the semiconductor device which examines about the quality of the property of a semiconductor device over two or more test conditions, especially, this invention changes two or more test conditions continuously, and relates to the testing device of the semiconductor device which creates the SHUMU plot which displays a quality judging result in the shape of a matrix.

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PRIOR ART

[Description of the Prior Art] High integration of a semiconductor device is attained by advance of semiconductor technology, for example, the storage capacity of a semiconductor memory is increasing by leaps and bounds in the past several years. If it is going to examine about the quality of the property of all test areas to the semiconductor device which has such a mass storage capacity, test time will also increase by leaps and bounds with increase of storage capacity. Development of the testing device of the semiconductor device which is a short time and judges the quality result of an exact property is strongly desired under such a background.
[0003] Hereafter, it explains, referring to a drawing about the testing device (it abbreviates to a circuit tester below) of the conventional semiconductor device. Drawing 10 is the block diagram showing the configuration of the important section of the conventional circuit tester.
[0004] In drawing 10 , a circuit tester 20 contains the input signal generating circuit 21, the output signal judging circuit 22, and CPU (arithmetic and program control)23. It connects with the input signal generating circuit 21 and the output signal judging circuit 22, and CPU23 controls actuation of each part. By the operating command outputted from CPU23, the input signal generating circuit 21 creates the predetermined data for a trial, and outputs the data for a trial to a semiconductor memory 1 through the signal input pin 2 grade of a semiconductor memory 1. It consists of control data which control each actuation of the store of the address data which specify the address of the memory cell in a semiconductor memory 1, the cell data stored in the memory cell, and a semiconductor memory 1, read-out, etc. as data for a trial. Here, generating circuits without the direct relation to the meaning of this invention, such as a cell data and control data, etc. omit illustration and explanation, and explain them below about address data at a detail.
[0005] The input signal generating circuit 21 contains an output circuit 211, a computing element 212, and a register 213. It connects with a computing element 212, the maximum of the address of data required for creation of address data, for example, all the test areas of a semiconductor memory 1, the minimum value, etc. are memorized beforehand, and a register 213 outputs predetermined data to a computing element 212 according to the operating command from CPU23. It connects with an output circuit 211, and a computing element 212 creates predetermined address data based on the data outputted from the register 213, and outputs them to an output circuit 211. It connects with the signal input pin 2 of a semiconductor memory 1, and an output circuit 211 inputs the inputted address data into a semiconductor memory 1. A semiconductor memory 1 memorizes the cell data separately transmitted in the predetermined memory cell based on the inputted address data.
[0006] Next, a semiconductor memory 1 outputs the written-in cell data to the output signal judging circuit 22 through read-out and the signal output pin 3. The output signal judging circuit 22 includes an input circuit 221 and the quality judging circuit 222. The cell data outputted from the semiconductor memory 1 is inputted into the quality judging circuit 222 through an input circuit 221. The quality judging circuit 222 is connected with a computing element 212, and the expected-value data showing the cell data which the input signal generating circuit 21 made memorize are inputted from a computing element 212. The quality judging circuit 222 compares expected-value data with the read cell data, and

judges the quality of a property. A judgment result is outputted to CPU23, and based on this judgment result, CPU23 displays a test result on a display or an airline printer (illustration abbreviation), and becomes possible [getting to know about the quality of the property of a semiconductor memory 1].

[0007] Next, the approach of the characteristic test of the semiconductor memory using the circuit tester 20 constituted as mentioned above is explained. One of the characteristic tests of a semiconductor memory has a SHUMU plot. A SHUMU plot examines by two or more test conditions to which two test condition parameters or three test condition parameters were changed at the predetermined spacing among some kinds of test condition parameters (for example, supply voltage, input timing of various signals, etc.), plots the quality judging result in the shape of [of two-dimensional or a three dimension] a matrix, and examines the property of a semiconductor memory.

[0008] An example of a SHUMU plot is shown in drawing 11 . The time amount which performs the quality judging of the data outputted as a test condition parameter from the supply voltage and the semiconductor memory which are given to a semiconductor memory is used. In drawing 11 , the time amount which performs the quality judging of the data which the supply voltage of 11 points is changed to 0.1V unit to 5.5V-4.5V for an axis of ordinate, and are outputted in supply voltage is changing the test condition of 16 points to the unit for 1ns for an axis of abscissa from 95ns till 110ns. Consequently, 11 points x 16 points = a trial is carried out by each test condition of 176 points, if a test result is "good", "*" will be displayed on that point, and if "poor", it is leaving in the null. By displaying as a SHUMU plot shown in drawing 11 , it becomes possible to recognize the quality of the test result to two or more test conditions at a glance.

[0009] Next, in order to create the above-mentioned SHUMU plot, the sequence of carrying out each test condition is explained. Drawing 12 is drawing showing the sequence of carrying out each test condition. As shown in drawing 12 , each test condition is carried out in sequence as an arrow head shows. First, after examining changing the 1st trial parameter of an axis of abscissa at the predetermined spacing after fixing the conditions of the 2nd trial parameter of an axis of ordinate and completing a trial to all the test conditions of an axis of abscissa, the test condition of the 2nd trial parameter of an axis of ordinate is changed at the predetermined spacing, and it examines similarly, and it repeats until a trial is completed about all test conditions.

[0010] Next, actuation of the conventional circuit tester which creates the SHUMU plot shown in drawing 12 is explained below. Drawing 13 is a flow chart explaining actuation of the conventional circuit tester. The flow chart shown in drawing 13 is beforehand memorized as a program by the storage in CPU23, and when CPU23 performs the program if needed, it is realized.

[0011] First, in step S21, CPU23 sets up the initial value of the test condition of an axis of ordinate.

[0012] Next, in step S22, CPU23 sets up the initial value of the test condition of an axis of abscissa.

[0013] Next, in step S23, the input signal generating circuit 21 and the output signal judging circuit 22 are ordered CPU23 so that it may examine by the set-up test condition, and it performs a trial.

[0014] Next, in step S24, the output signal judging circuit 22 judges the quality of a test result, and outputs a judgment result to CPU23. Based on the inputted quality judging result, CPU23 will shift to step S25, if a test result is "good", and if "poor", it will shift to step S26.

[0015] Next, it sets to step S25 and CPU23 displays "*" on the location which shows the predetermined test condition of a SHUMU plot. Since step S25 is skipped on the other hand when judged with it being "poor", nothing is displayed on a SHUMU plot.

[0016] Next, in step S26, it checks whether the trial has ended CPU23 to all the test conditions of an axis of abscissa. If the trial is not completed, in order to set up the test condition of the following axis of abscissa, it shifts to step S28. If the trial is completed, in order to set up the test condition of the following axis of ordinate, it shifts to step S27.

[0017] Next, in step S26, when it is judged that the test condition of an axis of abscissa is not completed and it shifts to step S28, CPU23 changes the test condition of an axis of abscissa into the following test condition, shifts to step S23, and repeats subsequent processings.

[0018] On the other hand, when it is judged that it ended about all the test conditions of an axis of abscissa in step S26, in step S27, it checks whether the trial to all the test conditions of an axis of

ordinate has ended CPU23. If the test condition of an axis of ordinate is not completed, and it carried out after that to step S29 and has ended to it in order to set up the following test condition, since the trial to all test conditions is completed, processing will be ended.

[0019] Next, when it is judged that the test condition of an axis of ordinate is not completed in step S27 and it shifts to step S29, CPU23 sets up initial value as a test condition of an axis of abscissa.

[0020] Next, in step S30, CPU23 changes the test condition of an axis of ordinate into the following test condition, shifts to step S23, and continues subsequent processings.

[0021] By the above actuation, a circuit tester 20 carries out the trial to all test conditions in the sequence of the test condition shown in drawing 12 , and becomes possible [creating the SHUMU plot showing the quality judging result of each test condition].

[0022] Next, the trial to all test conditions is performed as mentioned above, and a SHUMU plot is not created, but by examining in predetermined sequence explains below creation of the SHUMU plot by the binary search technique which can shorten test time. Drawing 14 is drawing explaining the test procedure by the binary search technique which used the conventional circuit tester.

[0023] As shown in drawing 14 , the 1st trial parameter is taken along an axis of abscissa, and the 2nd trial parameter is taken along an axis of ordinate. First, after fixing the 2nd trial parameter of an axis of ordinate to predetermined conditions, it examines by the test condition at the left end of the 1st trial parameter of an axis of abscissa. Next, it examines to the same 2nd trial parameter by the test condition at the right end of the 1st trial parameter of an axis of abscissa. The result of the test condition shown by the arrow head 2 serves as "good" ("*"), and that the result of the test condition shown by the test result and the arrow head 1 is "poor" (null), and when both test judging results differ, both middle point is examined. Here, the next trial is performed as a middle test condition by the test condition shown by the arrow head 3. When a test result is "good" at this time, the next trial is performed by the test condition between the test condition shown by the arrow head 1, and the test condition shown by the arrow head 3, for example, the conditions shown by the arrow head 4. When the test result in the test condition shown in an arrow head 4 is "poor", the next trial is performed by the test condition shown by the arrow head 5 which it is between the test condition shown by the arrow head 4, and the test condition shown by the arrow head 3. Since between the test condition shown by the arrow head 4 and the test conditions shown by the arrow head 5 serves as the boundary point of good/defect when the test result of the test condition shown by the arrow head 5 is "good", "*" is plotted into the part of the test condition shown by the arrow head 5.

[0024] Since the boundary point of good/defect can be specified without examining to all test conditions by examining by the test condition in the meantime when the binary search technique examines by two different test conditions as stated above, and test results differ, it becomes possible to shorten test time. For example, to nine test conditions, by examining by five test conditions, the boundary point of good/defect can be specified and test time is shortened by 5/9 in drawing 14 . By examining the above-mentioned processing to each test condition of the 2nd trial parameter, the whole test time can be shortened similarly and it becomes possible to create a SHUMU plot at a high speed.

[0025] Next, actuation of the conventional circuit tester by the above-mentioned binary search technique is explained. Drawing 15 is a flow chart explaining actuation of the conventional circuit tester by the binary search technique.

[0026] First, in step S31, CPU23 sets up initial value as a test condition of an axis of ordinate.

[0027] Next, in step S32, CPU23 performs the subroutine which performs test activation by the binary search technique. The subroutine of the test activation by the binary search technique is processed as follows.

[0028] First, in step S35, it examines by the test condition N which shows "good" as a quality judging result, and the test condition M which shows a "defect."

[0029] Next, in step S36, it examines by the test condition L of the midpoint of a test condition N and a test condition M.

[0030] Next, in step S37, the quality judging in the test condition L of a midpoint is performed. When a judgment result is "poor", it shifts to step S41, and in the case of "good", it shifts to step S38.

[0031] When judged with "good" at step S37, in step S38, a test condition N is transposed to a test condition L.
[0032] On the other hand, in step S37, when it is judged that it is "poor", in step S41, a test condition M is transposed to a test condition L.
[0033] By the above processing, the boundary point of good/defect will exist between a test condition N and a test condition M.
[0034] Next, in step S39, it checks whether a test condition N and a test condition M are ****** test conditions. Since the boundary point of good/defect can be specified when it is a ****** test condition, it shifts to step S40. If it is not a ****** test condition, since the boundary point of good/defect may exist between a test condition N and a test condition M, it will shift to step S36 and will examine again about the test condition L of a midpoint.
[0035] Next, in step S40, the point of "good" used as the boundary point of good/defect is plotted. Without examining to all test conditions, the test condition used as the boundary point of good/defect can be specified, and the above processing enables it to create a SHUMU plot at a high speed.

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EFFECT OF THE INVENTION

[Effect of the Invention] It is the test condition which included the test condition from which there are few test conditions and the quality of a property changes based on the quality result of the property acquired by the 1st trial means in the testing device of the semiconductor device of this invention, and since the trial to all test areas is performed, it becomes more possible rather than examining to two or more test conditions of all shortening test time sharply. Moreover, it becomes possible [the 1st trial means] to grasp the property correctly also with the semiconductor device from which the quality of a property changes intricately, since the trial is performed to all test conditions. Consequently, it becomes possible a high speed and to examine the quality of the property of a semiconductor device correctly irrespective of the property of a semiconductor device.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the conventional circuit tester is constituted as mentioned above, in order to extract a SHUMU plot as a characteristic test, the trial needed to be repeated to all the test conditions set as the axis of ordinate and the axis of abscissa, and there was a trouble that test time became very long. For example, supposing it examined all test areas by the predetermined test condition in the case of the semiconductor memory of 16Mbit, about 4.6 hours was required and very huge time amount was needed. Moreover, this test time increases by leaps and bounds with the increment in the capacity of a semiconductor memory, and becoming a problem bigger future still is expected.
[0037] Moreover, in the binary search technique currently developed as an approach of shortening test time, there was a trouble that it could not be used to the semiconductor device in which the property that the boundary point of good/defect exists more than plurality is shown. The SHUMU plot at the time of examining the semiconductor memory which has two or more boundaries of good ("*")/defect (null) in drawing 16 is shown. As shown in drawing 16 , when there are two or more boundaries of good/defect, in order to detect only one boundary, other boundaries will be disregarded by the binary search technique. The SHUMU plot at the time of examining the semiconductor memory which has the property shown in drawing 17 at drawing 16 by the binary search technique is shown. Since, as for the boundary of good/defect, only one was detected and the other boundary points were not detected so that clearly from drawing 17 , the quality judging result in which it completely made a mistake was displayed, and there was a problem that exact evaluation was unrealizable.
[0038] This invention is for solving the above-mentioned technical problem, and it aims at offering a high speed and the testing device of a semiconductor device which can examine the quality of the property of a semiconductor device correctly irrespective of the property of a semiconductor device.

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MEANS

[Means for Solving the Problem] In the 1st test area whose testing devices of the semiconductor device of this invention are a part of all test areas of a semiconductor device A 1st trial means to examine about the quality of the property of a semiconductor device over two or more test conditions, In a decision means to determine the 2nd test condition which is a part of two or more test conditions based on the quality result of the property acquired by the 1st trial means including the 1st test condition from which the quality of a property changes at least, and all the test areas of a semiconductor device A 2nd trial means to examine about the quality of the property of a semiconductor device over the 2nd test condition determined by the decision means is included.

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OPERATION

[Function] In the testing device of the semiconductor device of this invention, since it examines about the quality of the property of a semiconductor device to two or more test conditions of all in the 1st test area which is a part of all test areas, a perfect quality test result can be obtained. Since the 2nd test condition which is a part of two or more test conditions is determined based on this test result including the 1st test condition from which the quality of a property changes, the 2nd test condition has few those numbers than all test conditions, and turns into a test condition including the test condition from which the quality of a property surely changes. All test areas are examined about the quality of the property of a semiconductor device over this 2nd test condition.

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EXAMPLE

[Example] It explains referring to a drawing hereafter about the testing device (a circuit tester is called below like the conventional example) of the semiconductor device which is one example of this invention. Drawing 1 is the block diagram showing the configuration of the important section of the circuit tester of one example of this invention.
[0042] In drawing 1 , a circuit tester 10 contains the input signal generating circuit 11, the output signal judging circuit 12, CPU (arithmetic and program control)13, and the judgment result storage memory 14. It connects with the input signal generating circuit 11, the output signal judging circuit 12, and the judgment result storage memory 14, respectively, and CPU13 controls actuation of each part. The input signal generating circuit 11 answers the command signal of operation outputted from CPU13, creates the data for a trial, and inputs them into a semiconductor memory 1 through the input signal pin 2. As data for a trial, it consists of cell datas stored in the address data and the predetermined memory cell which specify the address of the memory cell in a semiconductor memory 1 as usual. Although a cell data etc. is inputted into a semiconductor memory 1 like the conventional circuit tester, since the meaning of this invention does not have direct relation, the generating circuit of a cell data etc. omits the explanation while omitting illustration.
[0043] A semiconductor memory 1 outputs the cell data memorized based on the data for a trial outputted from the input signal generating circuit 11 to the output signal judging circuit 12 through read-out and the signal output pin 3. The output-signal judging circuit 12 compares the inputted cell data with the expected-value data outputted from the input signal generating circuit 11, and outputs the judgment result of a quality to the judgment result storage memory 14 and CPU13. The judgment result storage memory 14 memorizes the judgment result of the quality outputted from the output signal judging circuit 12, and outputs it to CPU13 if needed.
[0044] The input signal generating circuit 11 contains an output circuit 111, a computing element 112, the 1st register 113, the 2nd register 114, and a change-over switch 115. The 1st register 113 is storing data required to generate the input signal for examining all the memory space of a semiconductor memory 1. For example, they are the maximum of the address corresponding to all the test areas of a semiconductor memory 1, the minimum value, etc. The 2nd register 114 is storing data required to generate the input signal for examining a part of memory capacity of a semiconductor memory 1. For example, they are the maximum of the address corresponding to the predetermined field of a test area, the minimum value, etc. A change-over switch 115 switches connection between the 1st register 113 and the 2nd register 114, and a computing element 112. That is, when examining all the test areas of a semiconductor memory 1, the 1st register 113 is specified and the data corresponding to all test areas are outputted to a computing element 112. Moreover, when examining a part of test area, the 2nd register 114 is connected, and the data corresponding to a predetermined test area are outputted to a computing element 112. A computing element 112 creates predetermined address data based on the data inputted from the 1st register 113 or the 2nd register 114, and outputs them to an output circuit 111. After an output circuit 111 operates the inputted address data orthopedically to a predetermined wave, it is outputted to a semiconductor memory 1 through the signal input pin 2. Data for a trial other than the

above-mentioned address data are created like the conventional circuit tester, and are inputted into a semiconductor memory 1. The output signal judging circuit 12 includes an input circuit 121 and the quality judging circuit 122. The semiconductor memory 1 which memorized the outputted cell data outputs the memorized cell data to an input circuit 121 through read-out and the signal output pin 3 again from the input signal generating circuit 11. The read cell data is outputted to the quality judging circuit 122 through an input circuit 121. The expected-value data in which the cell data memorized from the computing element 112 is shown are outputted to the quality judging circuit 122, this expected-value data is compared with the inputted cell data, and the quality of a property is judged. The quality judging circuit 122 outputs a judgment result to CPU13, when the judgment result of a quality is a thing to all test areas, and when it is a part of test area, it outputs a judgment result to the judgment result storage memory 14. The judgment result storage memory 14 memorizes the judgment result of some qualities of a test area, and CPU13 discriminates the boundary point of good/defect from which a property changes to good or a defect from the memorized judgment result. Based on the identified boundary point, CPU13 sets up a predetermined test condition including the test condition from which the quality of a property changes, and it orders it it so that all test areas may be examined by the test condition to the input signal generating circuit 11.

[0045] Next, actuation of the circuit tester constituted as mentioned above is explained to a detail. Drawing 2 is a flow chart explaining actuation of a circuit tester.

[0046] First, in step S1, CPU13 sets up data required to generate the input signal which examines the 1st predetermined test area which is a part of all test areas to the 2nd register 114 at the same time it sets up data required to generate the input signal which examines all the test areas of a semiconductor memory 1 to the 1st register 113. What is necessary is just to set up the minimum field in the field which shows the rough property of the semiconductor device examined as the 1st test area. An example of the 1st test area is shown in drawing 3 . As shown in drawing 3 , for example, when the storage capacity of a semiconductor memory 1 is 64Mbit, the part of 1Kbit of the lower address shown with the slash can be used as the 1st test area. Therefore, what is necessary is to set the value which accesses all the record sections of 64Mbit to the 1st register 113, and just to set the value which accesses only the part of 1Kbit of a lower address to the 2nd register 114.

[0047] Next, the trial to the 1st test area is performed in step S2. It is ordered CPU13 so that the 2nd register 114 side may be connected to a change-over switch 115, and predetermined data are outputted to a computing element 112 from the 2nd register 114. A computing element 112 outputs the calculated address data to a semiconductor memory 1 through an output circuit 111. Moreover, data for a trial, such as a cell data, are also inputted into a semiconductor memory 1 at coincidence. A semiconductor memory 1 outputs the cell data which read the memorized cell data to the quality judging circuit 122 through read-out and an input circuit 121 again. The quality judging circuit 122 compares the expected-value data of the cell data outputted from a computing element 112 with the read cell data, and judges the quality of a property.

[0048] Next, in step S3, the quality judging circuit 122 outputs the judgment result of a quality to the judgment result storage memory 14. The inputted judgment result is made to correspond with a SHUMU plot and the location of the shape of a matrix it was made to correspond, and the judgment result storage memory 14 memorizes it.

[0049] Next, in step S4, it checks whether the trial of all the test conditions over the 1st test area has ended CPU13. If the trial is not completed, after shifting to step S11 and changing into the following test condition, it shifts to step S2 and a trial is performed again. If the trial is completed, it will shift to step S5. By performing the above-mentioned processing, it becomes possible to examine the property of the outline of a semiconductor memory 1 comparatively for a short time. Here, since 1/64 of the test areas of all test areas are examined as the 1st test area, test time drops to 1/64 of the test time of all test areas.

[0050] Next, in step S5, CPU13 searches the test condition from which a property serves as the boundary point of good/defect which changes to good or a defect based on the quality judging result memorized by the judgment result storage memory 14. The SHUMU plot showing an example of the test result of the 1st test area in drawing 4 is shown. As shown in drawing 4 , it is stored in the main

storage (illustration abbreviation) which is made to correspond to the test condition of each boundary point which changes from it being "poor" (null) to "good" ("*") with the location on a matrix, and has it in the interior of CPU13. For example, if it says in a matrix-like location, the boundary point P1 is the 1st of an axis of ordinate, and will call it the 4th of an axis of abscissa. Since the data about these boundary points are memorized in main storage, they can access a high speed. Moreover, although drawing 4 shows the SHUMU plot in case the number of boundaries is one, since the trial is performed to all test conditions even when there are two or more boundaries, it is possible to detect all boundaries correctly. The above processing enables it to detect the data about the boundary point of perfect good/defect in the 1st test area which is a part of all test areas.

[0051] Next, in step S6, a test area is switched to all test areas. CPU13 orders so that a test area may be switched to the input signal generating circuit 11 from the 1st test area to all test areas. In the input signal generating circuit 11, a change-over switch 115 switches connection to the 1st register 113 from the 2nd register 114. Consequently, the address data outputted from a computing element 112 turn into address data corresponding to all test areas.

[0052] Next, in step S7, CPU13 sets up initial value as a test condition of an axis of ordinate.

[0053] Next, in step S8, CPU13 performs the subroutine which measures near the boundary point.

[0054] The subroutine which measures near the boundary point is explained below. It is possible that the boundary point of the good/defect of the property searched for at step S5 changes somewhat with test areas with the property of a semiconductor memory 1. Therefore, by examining to the test condition of several points before and after the boundary point of the good/defect searched for, the test condition in all test areas can detect the boundary point of good/defect to all test areas, and can obtain an exact quality judging result. The width of face of a test condition before and after inserting the boundary point is determined in consideration of dispersion in the property of the semiconductor device examined, and in consideration of a common semiconductor memory, an exact quality judging result shall be obtained and it shall examine to the test condition of three points here before and after the boundary point as a value with few test conditions.

[0055] Drawing 5 is drawing explaining the test procedure by this example. As shown in drawing 5 , the point which went to left-hand side 3 point focusing on the boundary point is made into a test condition L, and the point which went to right-hand side 3 point is made into a test condition R. When only the one boundary point exists in before the test condition L blank test conditions R, it examines by the predetermined test condition one by one to a boundary point side from the side judged that is "poor" as a quality judging result. If at least one cel of a defect is discovered in a test area, since the trial of a quality judging will stop a trial at the time and will judge the test result to the test condition as "poor" It is because the direction in the case of being "poor"er than the case of the "good" judged as a test result for the first time to be "good" is able to shorten the test time to one test condition sharply when the result of "good" comes out to all test areas.

[0056] Moreover, when other boundary points exist among the test condition L blank test conditions R, a test condition L or a test condition R shall be set up so that the boundary point may not be included, and the side blank test from which the result of "good" is obtained as a quality judging result shall be started.

[0057] Hereafter, actual processing of the subroutine of measurement of near the boundary point is explained. First, in step S13, CPU13 accesses the information about the boundary point of the good/defect currently stored in self main storage, and after it specifies the first boundary point, it sets up the test condition which returned from the boundary point 3 point as a test condition L.

[0058] Next, in step S14, it checks whether CPU13 contains other boundary points between a test condition L and the boundary point. When other boundary points are not included, it shifts to step S18. When other boundary points are included, in order to change a test condition, it shifts to step S15.

[0059] Next, in step S15, CPU13 sets up the test condition of the point which progressed 3 point from the boundary point as a test condition R.

[0060] Next, in step S16, it checks whether CPU13 contains other boundary points between a test condition R and the boundary point. When other boundary points are not included, it shifts to step S18.

When other boundary points are included, in order to change a test condition, it shifts to step S17.
[0061] Next, in step S17, CPU13 changes a test condition L and a test condition R so that other boundary points may not be included among the test condition L blank test conditions R. Consequently, the one boundary point will surely exist in before the test condition L blank test conditions R.
[0062] Next, in step S18, the test condition started according to the above regulations from between the set-up test condition L blank test conditions R is set up, the test condition blank test is performed, and the boundary point is found.
[0063] Next, in step S19, it is checked whether all the boundary points have been found in CPU13. Since it is not necessary to continue the trial beyond this when all the boundary points are found, processing by the subroutine is ended and it shifts to step S9. Since it is necessary to examine succeedingly and to find the boundary point when all the boundary points are not found, it shifts to step S20.
[0064] Next, in step S20, CPU13 changes the test condition of an axis of abscissa into the test condition containing the following boundary point, and in order that it may return to step S13 and may find the following boundary point, it continues subsequent processings.
[0065] After processing of the subroutine which measures near [above] the boundary point is completed, in step S9, CPU13 displays a test result on a display or an airline printer (illustration abbreviation) as a SHUMU plot.
[0066] Next, in step S10, it checks whether the trial has ended CPU13 to all the test conditions of an axis of ordinate. If the trial is completed to all the test conditions of an axis of ordinate, processing is ended and the trial is completed to no test conditions of an axis of ordinate, it will shift to step S12.
[0067] Next, in step S12, CPU13 changes the test condition of an axis of ordinate 1 point, shifts to step S8, and continues subsequent processings.
[0068] Based on the information about the boundary point of the good/defect extracted in the 1st test area which is a part of test area, the test condition near the boundary point can be set up, a trial can be performed to all test areas only by the test condition, and the above actuation enables it to shorten test time sharply. Moreover, since the information about the boundary point is created based on the result of having examined to all test conditions, it can grasp the property correctly also in the semiconductor memory which has a property containing two or more boundary points. Therefore, it becomes possible a high speed and to examine the quality of the property of a semiconductor device correctly irrespective of the property of a semiconductor device.
[0069] The SHUMU plot acquired with this equipment by drawing 6 is shown. In drawing 6 , the boundary point of the good/defect of a judgment result is shown by "*." It turns out that the SHUMU plot by this equipment has detected all the boundary points correctly to two or more boundary points so that clearly from drawing 6 . Moreover, drawing showing the point which actually examined to drawing 7 is shown. In drawing 7 , in "F", a defect and "P" show "good" and "*" shows the boundary point, respectively. It is possible by examining to the test condition of several points to become possible to extract the one boundary point and to reduce the number of required test conditions sharply so that clearly from drawing 7 .
[0070] The relation between the device capacity of a semiconductor memory and the extraction time amount of a SHUMU plot is shown in drawing 8 . In drawing 8 , the conventional circuit tester [according / a broken line / to the binary search technique] according [a continuous line] to the circuit tester of this example and the alternate long and short dash line show the conventional circuit tester, respectively. In this example, it is possible to extract a SHUMU plot by the time amount of about 1/8 compared with the conventional circuit tester so that clearly from drawing 8 . Moreover, compared with the binary search technique, it realizes by almost equivalent time amount, and it is possible to extract an exact SHUMU plot by extraction time amount equivalent to the binary search technique also to the semiconductor device which has two or more boundary points of the good/defect which was not able to be evaluated by the binary search technique.
[0071] Although the above-mentioned example described to the predetermined value of an axis of ordinate on the assumption that at least one boundary point existed When it differs from the judgment

result from which only the two-poles value of the 1st parameter of an axis of abscissa was examined, and the judgment result was obtained by the 1st test area when the boundary point did not exist If it is made to examine until it discovers the new boundary point, it will become possible to apply also to the test condition which does not contain the boundary point.

[0072] Moreover, although the judgment result storage memory 14 was formed and the judgment result was made to memorize in the above-mentioned example, the same effectiveness can be acquired even if it makes the main storage or other storage in CPU13 memorize. Moreover, if a free area is in the judgment result storage memory 14, even if it stores in the field, after acquiring the same effectiveness or eliminating the data of the judgment result storage memory 14, you may make it store the information about the boundary point, although the information about the boundary point searched from the data in the judgment result storage memory 14 was memorized in the main storage in CPU13 in the above-mentioned example.

[0073] Moreover, by not forming the 2nd register 114 but using for example, a diagonal pattern etc. based on the data about all the test areas currently stored in the 1st register 113, although the data about the 1st predetermined test area were stored in the 2nd register 114 in the above-mentioned example, even if it devises the sequence which accesses the memory cell in a semiconductor memory 1, it becomes possible to judge a property comparatively for a short time. Drawing 9 is drawing showing a diagonal pattern. In this case, the memory cell of the slash shown in drawing 9 turns into a memory cell which examines as the 1st record section. Its property of the semiconductor device measured is not uniform to all test areas, and such a diagonal pattern is effective especially when the property of all test areas cannot be expressed with the test result of a predetermined partial part.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the configuration of the important section of the testing device of the semiconductor device of one example of this invention.
[Drawing 2] It is the flow chart which shows actuation of the testing device of the semiconductor device of one example of this invention.
[Drawing 3] It is drawing showing an example of the 1st test area.
[Drawing 4] It is drawing showing an example of the test result of the 1st test area.
[Drawing 5] It is drawing explaining the test procedure of the testing device of the semiconductor device of one example of this invention.
[Drawing 6] It is drawing showing the quality result obtained by the testing device of the semiconductor device of one example of this invention.
[Drawing 7] It is drawing showing the point which actually examined with the testing device of the semiconductor device of one example of this invention.
[Drawing 8] It is drawing showing the relation between device capacity and the extraction time amount of a SHUMU plot.
[Drawing 9] It is drawing showing a diagonal pattern.
[Drawing 10] It is the block diagram showing the configuration of the important section of the testing device of the conventional semiconductor device.
[Drawing 11] It is drawing showing an example of a SHUMU plot.
[Drawing 12] It is drawing explaining the test procedure by the testing device of the conventional semiconductor device.
[Drawing 13] It is the flow chart which shows actuation of the testing device of the conventional semiconductor device.
[Drawing 14] It is drawing explaining the test procedure by the binary search technique using the testing device of the conventional semiconductor device.
[Drawing 15] It is a flow chart explaining actuation by the binary search technique using the testing device of the conventional semiconductor device.
[Drawing 16] It is drawing showing the quality judging result at the time of examining a semiconductor device with two or more boundaries of good/defect.
[Drawing 17] It is drawing showing the quality judging result at the time of examining the semiconductor device which has the property shown in drawing 16 by the binary search technique.
[Description of Notations]
10 Circuit Tester
11 Input Signal Generating Circuit
12 Output Signal Generating Circuit
13 CPU
14 Judgment Result Storage Memory
111 Output Circuit

112 Computing Element
113 1st Register
114 2nd Register
115 Change-over Switch
121 Input Circuit
122 Quality Judging Circuit

[Translation done.]

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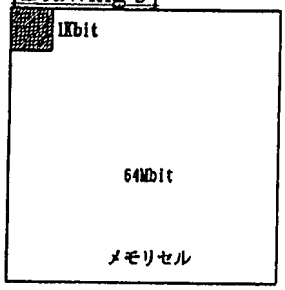
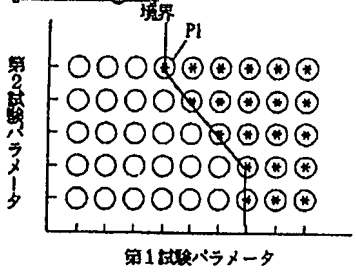
DRAWINGS

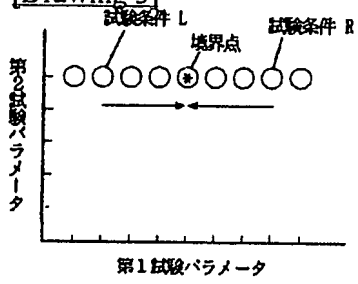
[Drawing 3]



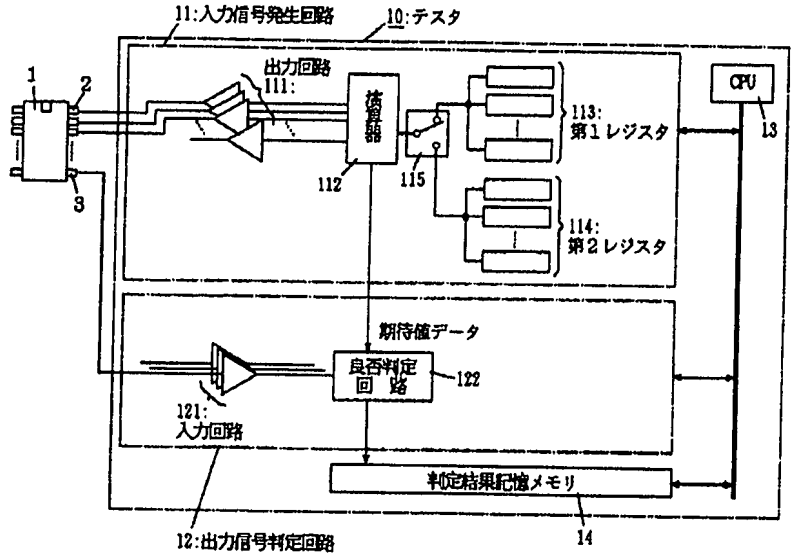
[Drawing 4]



[Drawing 5]

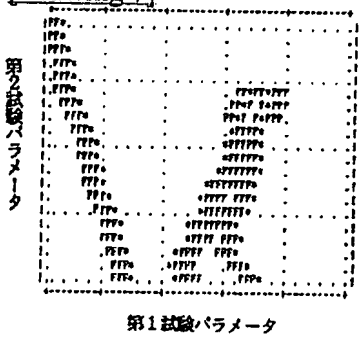


[Drawing 1]

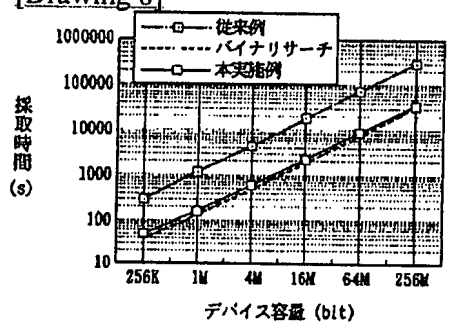


[Drawing 6]

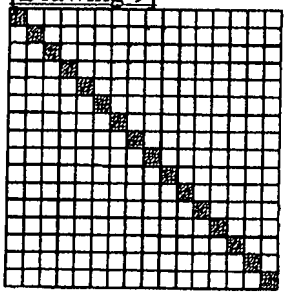
[Drawing 7]



[Drawing 8]

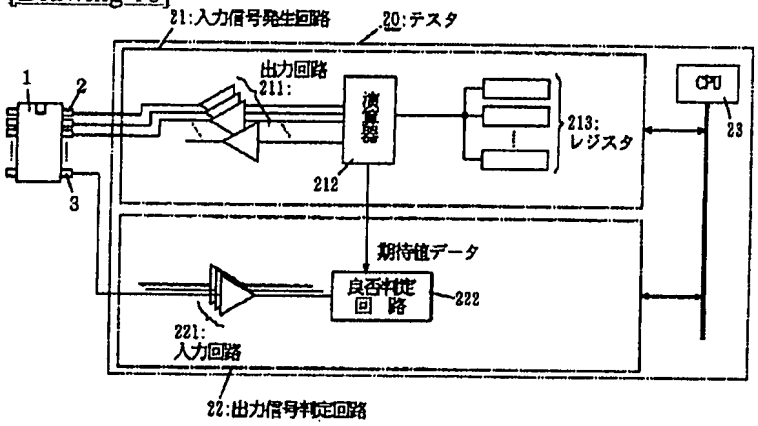


[Drawing 9]

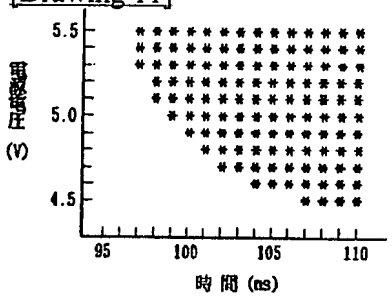


ダイアゴナル・パターン

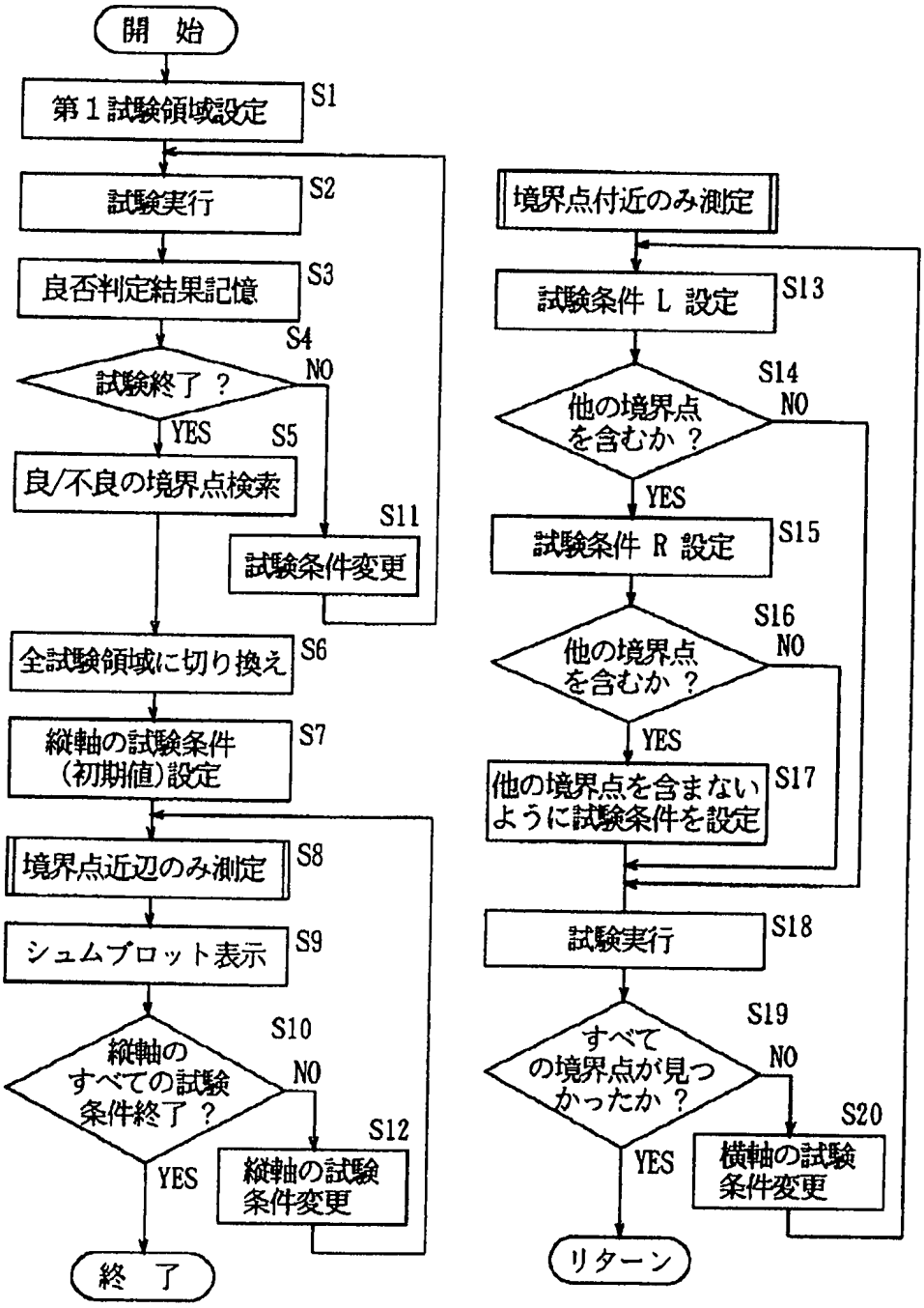
[Drawing 10]



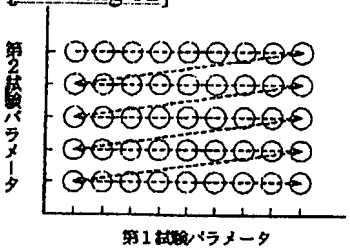
[Drawing 11]



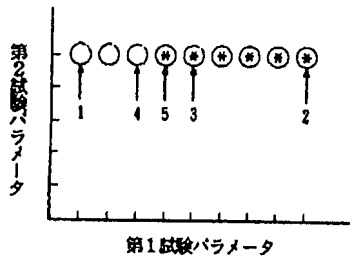
[Drawing 2]



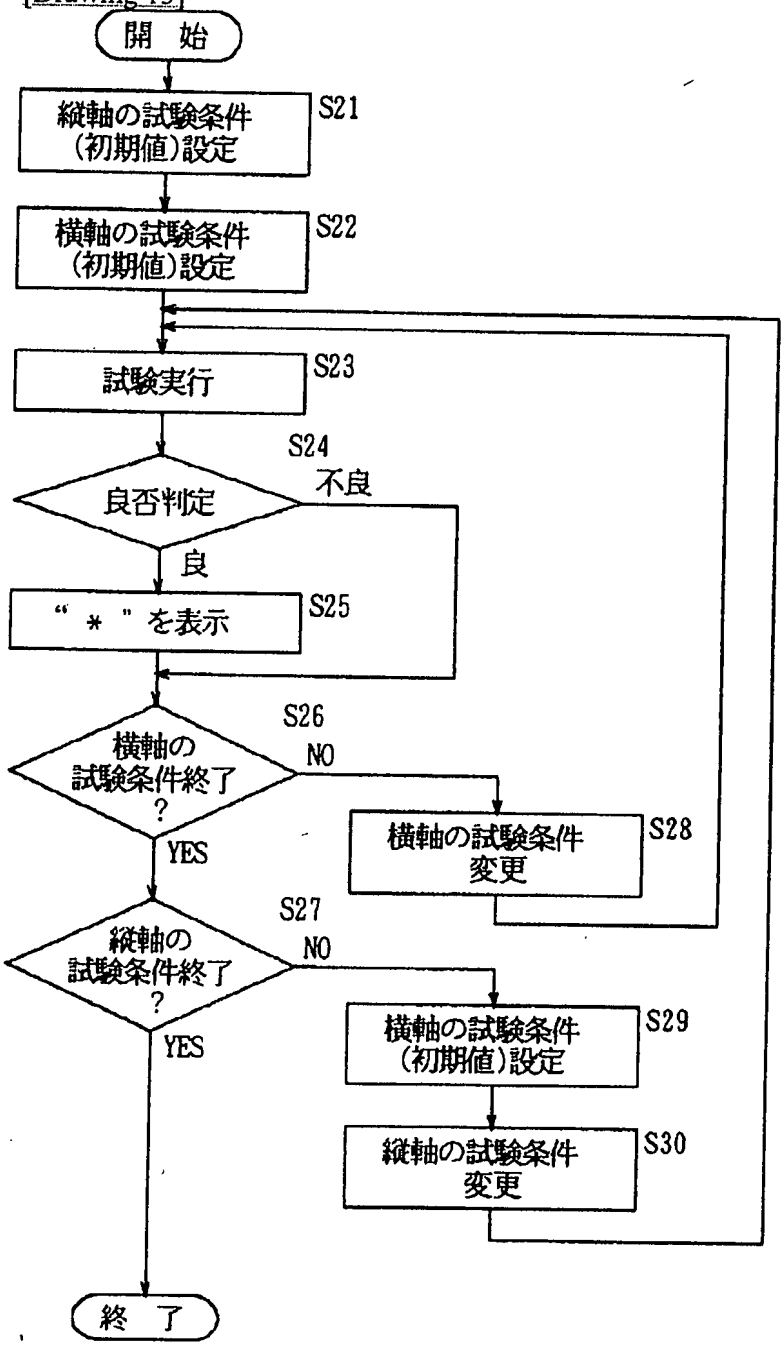
[Drawing 12]



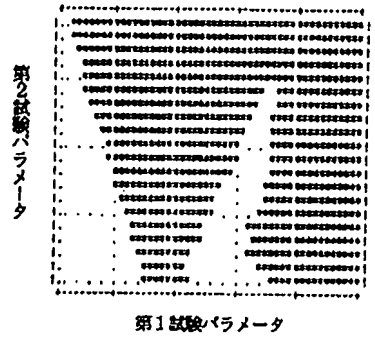
[Drawing 14]



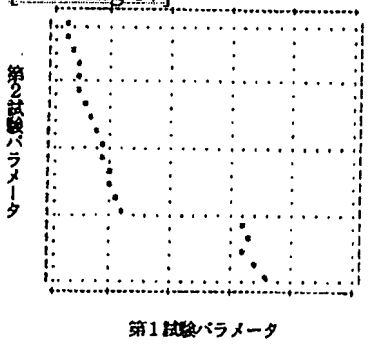
[Drawing 13]



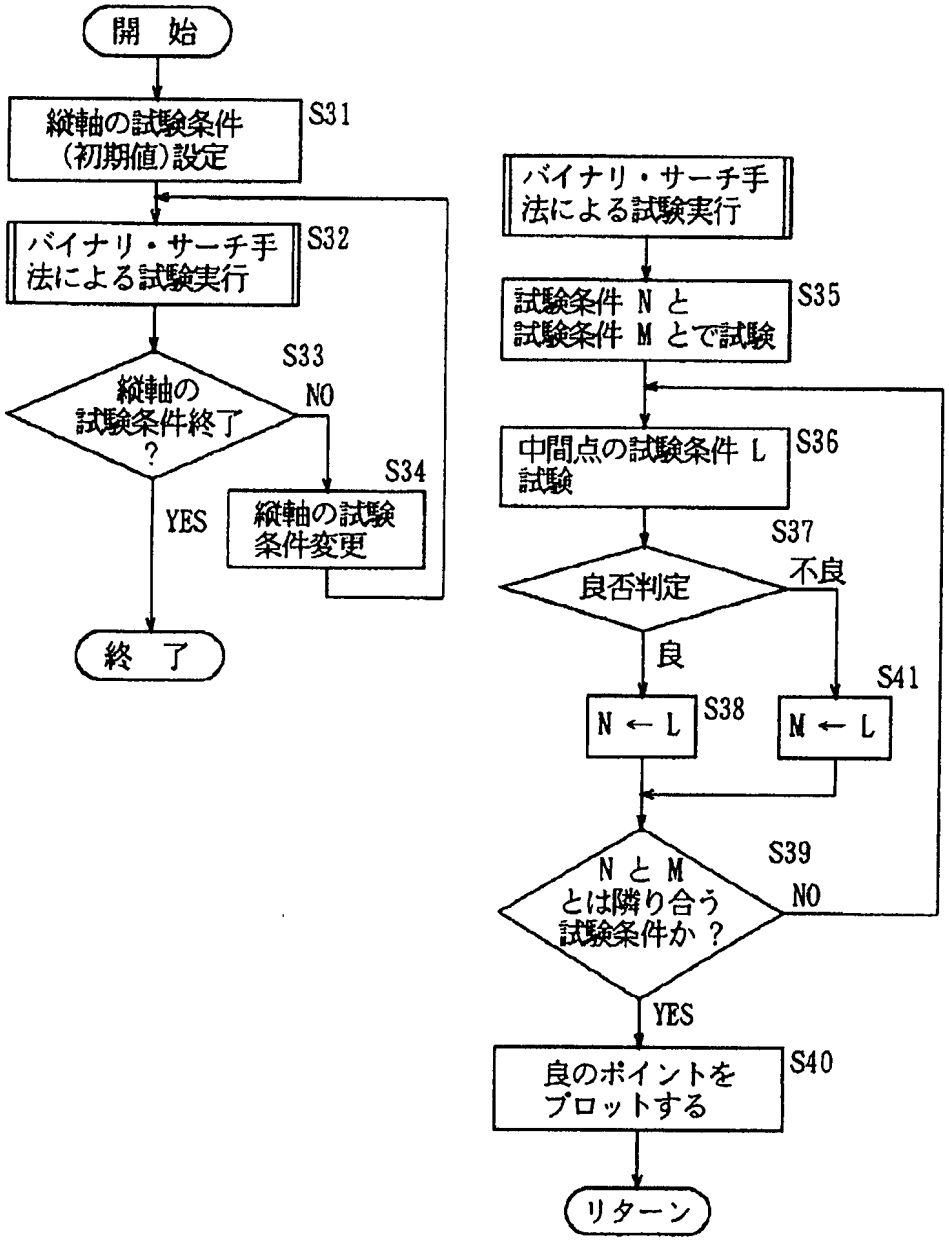
[Drawing 16]



[Drawing 17]



[Drawing 15]



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